



INTRODUCTION:

This application note describes an opamp-based bias circuit to set the bias current for low-noise amplifiers designed with LN180 or LN240 low-noise 0.15um PHEMT devices. These devices are based on a quasi-enhancement mode process that has very low pinch-off voltage V_p of -0.3V typ. Hence the V_g settings for typical operating bias currents (15 to 30 mA) can be near 0 volts +ve or -ve, due to normal process variations. This bias network will set the bias current & V_g automatically irrespective of the required V_g being +ve or -ve for that bias current by using resistive feedback from the drain bias input.

DESCRIPTION:

Typical drain voltage bias for LNAs is 2 to 4 V. In most applications supply voltage of + 5V and - 5V is available. Hence by dropping the voltage using a resistor between the +ve supply and the V_{dd} input of the LNA, the feedback voltage can be compared with a reference voltage set at the Opamp inverting input. The recommended circuit is shown in Figure 1. It utilizes a standard low-cost Opamp TL081ID from STMicroelectronics with 4 resistors in a feedback configuration to set the V_g gate voltage of the PHEMT. The negative supply voltage for the Opamp can be -3 to -5V and must be more negative than V_p of the LN device. The low-impedance output of the Opamp will allow sinking of PHEMT gate leakage currents with negligible change in V_g and drain bias currents.

DESIGN APPROACH:

- 1) Assuming the value of V_{POS} , I_{dd} , and V_{dd} are known, the I_{dd} can be set as follows:

$$I_{dd} = (V_{POS} - V_{dd}) / R_d$$

- 2) Calculate $R_{dd} = (V_{POS} - V_{dd}) / I_{dd}$

- 3) The reference voltage $V_{ref} (=V_{dd})$ for the Opamp is derived from V_{POS} using a voltage divider by determining the resistor ratio as follows

$$\text{ratio} = R_4 / (R_3 + R_4) = V_{ref} / V_{POS}$$

- 4) Choose some high value for R_4 and calculate R_3 as follows: $R_3 = R_4 * (1 - \text{ratio}) / \text{ratio}$

Typical example:

$I_{dd} = 30 \text{ mA}$, $V_{dd} = V_{ref} = 3\text{V}$, $V_{POS} = 5\text{V}$, $V_{NEG} = -3 \text{ to } -5 \text{ V}$

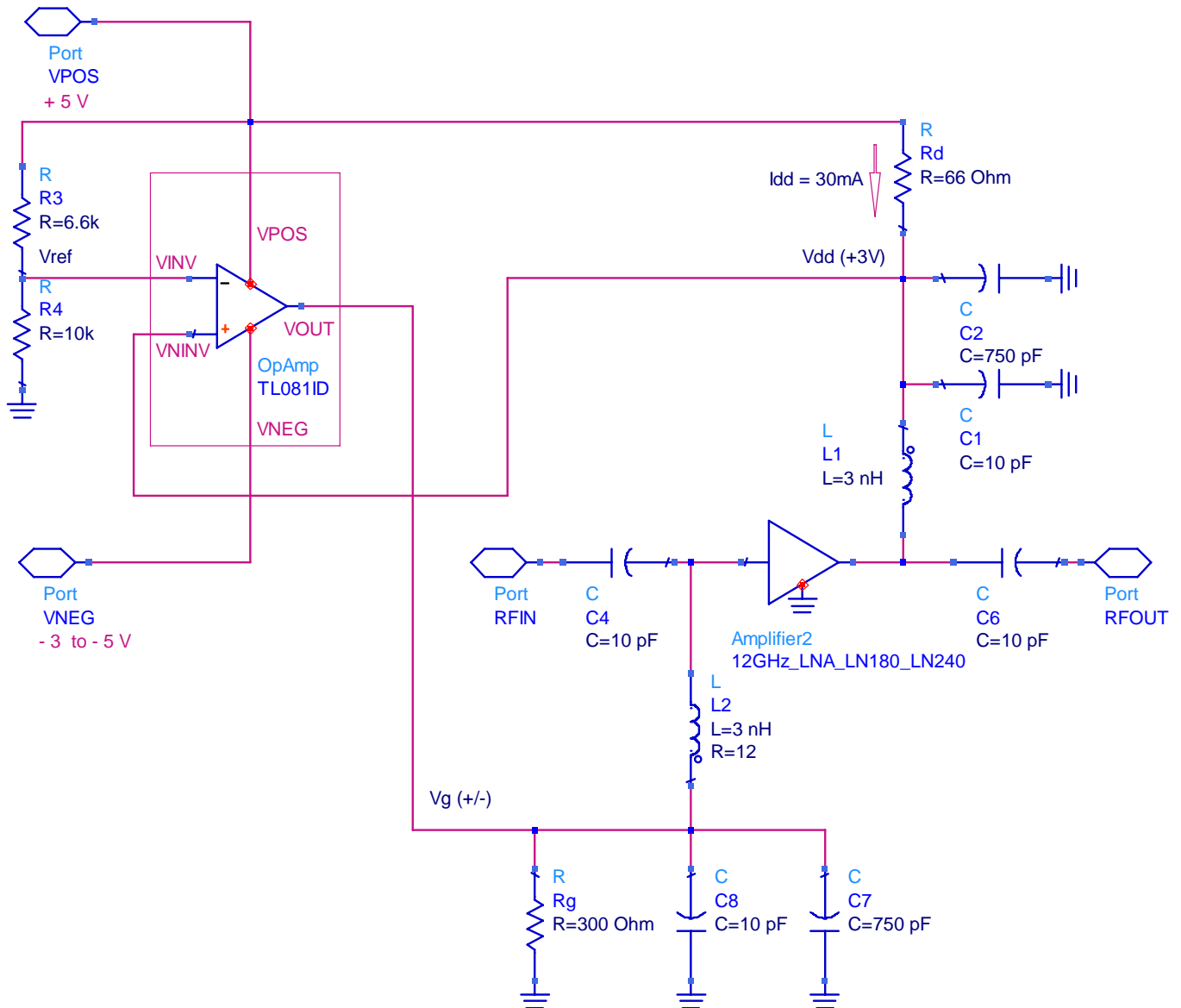
$R_d = (5 - 3) / 0.03 = 66.66 \text{ ohms}$. R_d must be chosen to handle the dissipated DC power of $2 \times 0.03 = 60\text{mW}$

$\text{ratio} = 3 / 5 = 0.6$

Choose $R_4 = 10\text{K}$, then $R_3 = 10\text{k} (1 - 0.6) / 0.6 = 6.66\text{k ohms}$

Figure 1

OPAMP BIAS APPLICATION SCHEMATIC FOR LN180/LN240 12GHz LNA



DESIGN ISSUES:

The bias circuit using Opamp must address several design issues which maybe important depending on the specific application.

- 1) **Opamp Stability:** The design must ensure opamp stability while the opamp drives the Vg input of the device gate. Typically gate bias will have large bypass capacitors and the chosen opamp must be capable of driving large capacitive loads without instability. With the opamp chosen for this example TL081ID, it was empirically determined that gate bypass capacitors need to be < 1000pF and requiring a shunt loading resistor Rg of < 500 ohms. Rg was empirically set at 300 ohms. The bypass capacitors on the drain bias input do not generally cause opamp stability problems but may have to be considered for complete analysis.
- 2) **Transient Response:** If the LNA is designed for applications where pulsed or transient RF signals, then the opamp bias circuit could affect the transient response and must be included in the analysis to check the settling time or any other time-dependent parameters.
- 3) **Signal Modulation:** Since the bias circuit is attached to +ve and -ve power supplies, any modulation of the DC voltages coming from the switching power supply and/or digital circuitry etc. can be injected into the amplifier from the gate voltage input and affect the amplifier operation when modulated signals are present. For very high modulation frequencies or large amplitudes, filtering of the positive and negative terminals of the opamp may be necessary to reduce the unwanted signals to an acceptable.
- 4) **Bias Accuracy:** The current setting accuracy is determined by the Rd value and VPOS value. It is better to choose Rd resistor with 1% rating. The % variation of Idd is directly proportional to % variation of VPOS value. The non-ideal opamp characteristics and voltage divider resistors R3 and R4 will also affect the accuracy of Idd but not as much. Other solutions can be implemented to mitigate these effects if required by the final design.
- 5) **Other Issues:** There maybe other considerations that require further study like the cost of the bias network, board space, power consumption, temperature performance and qualification for military and space requirements.

TYPICAL PERFORMANCE DATA WITH 12GHz DISCRETE LNA DESIGN:



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The opamp bias circuit shown in Figure 1 was implemented for a discrete 12GHz LNA design using LN240 device. The performance comparison of the LNA is shown in Table 1 & 2 using direct dual bias and with Opamp bias circuit. As can be seen there is almost no change in small-signal performance except for the P-1dB drop @ 11GHz where current increase vs drive gets limited due to feedback. The LNA was also power blasted with the Opamp bias circuit for 2 min duration with 12GHz CW input. The LNA could handle 13 dBm input with < 0.5 dB drop in P-1dB @ 12GHz and almost no degradation in Gain, Return loss and NF parameters.

Table 1: Data with Direct Dual Bias Vdd =3V, Idd = 30mA, Vg = + 0.039V

Freq (GHz)	S21 (dB)	S11 (dB)	S22 (dB)	NF(dB)	P-1(dBm)	Idd (mA)
11	13.4	-2.5	-13	0.74	15.5	37
12	12.2	-2.1	-12.2	0.84	14.7	32
13	11.1	-1.78	-10.3	0.98	15.2	31

Table 2: Data with Opamp Bias Vdd = 3.075 V, Idd = 30.5 mA, Vg (Opamp output) = + 0.045 V
 VPOS=+5V, VNEG=-5V, Vref= 3.078V, Rg = 300 ohm, I (Opamp) = 1.2 mA

Freq (GHz)	S21 (dB)	S11 (dB)	S22 (dB)	NF(dB)	P-1(dBm)	Idd (mA)
11	13.45	-2.5	-13	0.74	14.6	31.5
12	12.26	-2.08	-12.17	0.84	14.7	31.5
13	11.12	-1.75	-10.28	0.98	15.1	31