The MLA-0522A-87 is a partially matched single-stage broadband Low-Noise MMIC amplifier utilizing high-reliability low-noise GaAs PHEMT technology. The packaged MMIC is suited for Iridium Satellite Communications, Instrumentation, Wideband Systems and also many commercial wireless applications where low-noise figure and high-dynamic range is desirable. It has excellent gain 15 dB and Noise Figure 1.1 dB @ 1.6 GHz which is ideally suited for Iridium Satellite Band applications. P-1dB is 15 dBm and OIP3 is 30 dBm @ 1.6 GHz. It has partial input match and full output match on-chip providing flexibility to optimize NF performance using external input match. The bias current is adjustable with gate voltage down to 30mA. with good performance. Other package options are available. Contact factory for details.

FEATURES
- Wide Band: 0.2 GHz to 2.0 GHz
- NF (ext match): 0.9 dB @ 0.2 GHz, 1.0 dB @ 0.5 GHz, 1.1 dB @ 1.6 GHz, 1.2 dB @ 2.0 GHz
- P-1dB: 15 dBm
- OIP3: 33 dBm
- High Gain: 15 dB
- Bias Condition: VDD = 3V, IDD = 65mA
- Unconditionally Stable: 50 MHz to 7 GHz
- Narrow-Band Optimization with External Tuning
- Frequency Extension to 50 MHz with External Choke
- Surface-Mount Hermetic 8-Lead, 87 Package

APPLICATIONS
- Wide-band Communication Systems
- Commercial Wireless Systems
- Iridium Satellite Communications
- Test Instrumentation
- Surveillance Systems

DESCRIPTION
The MLA-0522A-87 is a partially matched single-stage broadband Low-Noise MMIC amplifier utilizing high-reliability low-noise GaAs PHEMT technology. The packaged MMIC is suited for Iridium Satellite Communications, Instrumentation, Wideband Systems and also many commercial wireless applications where low-noise figure and high-dynamic range is desirable. It has excellent gain 15 dB and Noise Figure 1.1 dB @ 1.6 GHz which is ideally suited for Iridium Satellite Band applications. P-1dB is 15 dBm and OIP3 is 30 dBm @ 1.6 GHz. It has partial input match and full output match on-chip providing flexibility to optimize NF performance using external input match. The bias current is adjustable with gate voltage down to 30mA. with good performance. Other package options are available. Contact factory for details.

ELECTRICAL SPECIFICATIONS: \( VDD=+3.0V, VG=0V, IDD=70mA, Ta=25\,^\circ C, ZO=50\,\text{ohm} \) (1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYPICAL DATA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency Range</td>
<td>Gain</td>
<td>0.2 - 1 GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.0 GHz</td>
</tr>
<tr>
<td></td>
<td>Gain Flatness</td>
<td>0.2 - 0.9 GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 - 2 GHz</td>
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<tr>
<td></td>
<td>Input Return Loss</td>
<td>0.2 GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 GHz</td>
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<tr>
<td></td>
<td></td>
<td>1.6 GHz</td>
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<tr>
<td></td>
<td></td>
<td>2 GHz</td>
</tr>
<tr>
<td></td>
<td>Output Return Loss</td>
<td>0.2 GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1.6 GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 GHz</td>
</tr>
<tr>
<td></td>
<td>Output P1dB</td>
<td>0.2 - 2 GHz</td>
</tr>
<tr>
<td></td>
<td>Output IP3 @ 0 dBm/tone, 1 MHz separation</td>
<td>0.2 GHz</td>
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<tr>
<td></td>
<td></td>
<td>0.5 GHz</td>
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<tr>
<td></td>
<td></td>
<td>1.6 GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 GHz</td>
</tr>
<tr>
<td></td>
<td>Noise Figure (Ext Input matched for 1.6 GHz)</td>
<td>0.2 GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.5 GHz</td>
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<tr>
<td></td>
<td></td>
<td>1.6 GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2 GHz</td>
</tr>
<tr>
<td></td>
<td>Operating Bias Conditions: VDD, IDD</td>
<td>VG = -0.04V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>65 V</td>
</tr>
<tr>
<td>Stability Factor K</td>
<td>0.05 to 7 GHz</td>
<td>&gt; 1</td>
</tr>
</tbody>
</table>

(1) All data is measured on 50 Ohm evaluation board with external input match, Bias Choke, Bypass and DC blocking caps. See application schematic and evaluation PCB layout.
TYPICAL RF PERFORMANCE: $VDD=+3.0V$, $VG=-0.04V$, $IDD=65mA$, $Ta=25\ C$, $ZO=50\ ohm$ (1)
Notes:

1) Please contact factory sales for additional information on external components and matching for improved performance.

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETERS</th>
<th>UNITS</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>Drain Voltage</td>
<td>V</td>
<td>6</td>
</tr>
<tr>
<td>IDD</td>
<td>Drain Current</td>
<td>mA</td>
<td>150</td>
</tr>
<tr>
<td>Pdiss</td>
<td>DC Power Dissipation</td>
<td>W</td>
<td>0.6</td>
</tr>
<tr>
<td>Pin max</td>
<td>RF Input Power</td>
<td>dBm</td>
<td>+17</td>
</tr>
<tr>
<td>Toper</td>
<td>Operating Case/Lead Temp Range</td>
<td>°C</td>
<td>-40 to +85</td>
</tr>
<tr>
<td>Tch</td>
<td>Channel Temperature</td>
<td>°C</td>
<td>150</td>
</tr>
<tr>
<td>Tstg</td>
<td>Storage Temperature</td>
<td>°C</td>
<td>-60 to 150</td>
</tr>
</tbody>
</table>

Exceeding any one of these limits may cause permanent damage.
MECHANICAL INFORMATION

87 Package Outline Drawing

Orientation Tab (PIN 1)

.070 MAX

.070 X .100 MIN.
GLASS FREE AREA

.005 ± .002

.000 +.003 /-.000
Coplanarity (lead foot may be up to
+.003 below bottom of package

.080

.085

.050

.196 .150

.015 ± .003 (8 places)

.000 +.003 /-.000
Coplanarity (lead foot may be up to
+.003 below bottom of package

.055 ± .005 (8 PLACES)

Case Bottom is Ground

.008 MIN. GLASS FREE AREA

.002

.020

.002

.032 MIN.

.057 MAX

.050

.150

Dimensions are in inches

Functional Diagram

N/C

N/C

GND

GND

RFIN

RFOUT

VC

VCC

MLA-0522A-87
0.2 GHz - 2.0 GHz Low-Noise MMIC Amplifier
Data Sheet
EVALUATION BOARD LAYOUT

MLA-0522A-87 APPLICATION BOARD

PARTS LIST:
R1: 3.3 ohm, 0603, 0.1W
R2: 000 ohm, 0603
R3: 000 ohm, 0603
C1: 1.0 pF AVX LOW-ESR 04023U1R0BAT2A
C4,C6: 120 pF AVX 04025A121JAT2A
C2,C3,C5,C7: 0.012 uF AVX 0402YC123KAT2A
L1: 56 nH, COILCRAFT 0603CS-56NXJL (High-Band)
390 nH, COILCRAFT 0603LS-391XJL (Wide-Band)
P1, P2: DC CONNECTOR TSM-105-01-SSV
J1, J2: RF CONNECTOR JOHNSON, 142-0701-841
U1: MLA-0522A-87, 8L, 87 HERMETIC PACKAGE

87 PACKAGE PIN LABEL/FUNCTION:
PIN 1: GND OR N/C
PIN 2: GND
PIN 3: RF INPUT
PIN 4: VG GATE BIAS INPUT
PIN 5: GND
PIN 6: RF OUT
PIN 7: VDD DRAIN BIAS INPUT
PIN 8: GND OR N/C

BACKSIDE: DC/RF GROUND

APPLICATION NOTES:

C1 MUST BE PLACED APPROX. 200MIL FROM THE LEAD 3 SOLDER JUNCTION ON THE 50 OHM MICROSTRIPLINE AS SHOWN AND LOCATION CAN BE TUNED FOR BEST INPUT RETURN LOSS AT 1.6 GHZ

R1 RESISTOR IS REQUIRED FOR DC/RF STABILITY

L1 SERVES AS RF CHOKE

C2, C3 ARE USED FOR DC BLOCKING

C4,C5, C6 & C7 SERVE AS BYPASS CAPS

87 PACKAGE BACKSIDE MUST BE SOLDERED WELL TO PCB GROUND VIAS FOR GOOD RF/DC GROUNDING

PACKAGE LEADS MUST BE SOLDERED STARTING FROM LEAD BEND JUNCTION

PCB MATERIAL: R04003C, 20MIL THICK, 2-LAYER, 1 OZ COPPER BOTH SIDES

BOARD SIZE: 1.45 x 1.45 in