FEATURES

- **Wide Band:** 0.2 to 2 GHz
- **NF (ext match):**
  - 0.2 GHz: 0.9 dB
  - 1.6 GHz: 0.95 dB
  - 2 GHz: 1.1 dB
- **P-1dB:** 16 dBm
- **OIP3:** 33 dBm
- **High Gain:** 16 dB
- **Bias Condition:** VDD = 3V, IDD = 70mA
- **50-Ohm On-chip Matching**
- **Unconditionally Stable from 50 MHz to 7 GHz**
- **Narrow-Band Optimization with External Tuning**
- **Frequency Extension to 50 MHz with External Choke**

APPLICATIONS

- **Wide-band Communication Systems**
- **Commercial Wireless Systems**
- **Iridium Satellite Communications**
- **Test Instrumentation**
- **Surveillance Systems**

DESCRIPTION

The MLA-0522A is a fully-matched single-stage broadband Low-Noise MMIC amplifier utilizing high-reliability low-noise GaAs PHEMT technology. This MMIC is ideally suited for Iridium Satellite Communications, Instrumentation, Wideband Systems and also many commercial wireless applications where low-noise figure and high-dynamic range is desirable. It has excellent gain 16 dB and Noise Figure 1.25 dB @ 1.6 GHz which is ideally suited for Iridium Satellite Band applications. Typical P-1dB is 16 dBm and OIP3 is 33 dBm @ 1.6 GHz. It has 50-ohm on-chip matching with flexibility to bypass on-chip match & optimize performance using external match. The bias current is adjustable with gate voltage down to 30 mA with good performance. Packaged options are available. Contact factory for further details.

**ELECTRICAL SPECIFICATIONS:** VDD=+3.0V, VG=0V, IDD=70mA, Ta=25 C, ZO=50 ohm

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>TYPICAL DATA</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>Gain Flatness</td>
<td>0.2 - 1 GHz</td>
<td>0.5</td>
<td>dB</td>
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<tr>
<td>Output Return Loss</td>
<td>0.5 GHz</td>
<td>12</td>
<td>dB</td>
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<tr>
<td>Output P1dB</td>
<td>0.2 - 1.8 GHz</td>
<td>16</td>
<td>dB</td>
</tr>
<tr>
<td>Output IP3</td>
<td>0.2 GHz</td>
<td>34</td>
<td>dB</td>
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<tr>
<td>Noise Figure</td>
<td>0.2 GHz</td>
<td>1.1</td>
<td>dB</td>
</tr>
<tr>
<td>Operating Bias Conditions: VDD</td>
<td>VDD=+3V, VG=0V</td>
<td>+3</td>
<td>mA</td>
</tr>
<tr>
<td>Stability Factor K</td>
<td>50 MHz to 7 GHz</td>
<td>&gt; 1</td>
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(1) All data is measured on 50 Ohm carrier with external bias choke, bypass and DC blocking caps. See evaluation assembly diagram.
TYPICAL RF PERFORMANCE: $VDD=+3.0V$, $VG=0V$, $IDD=70mA$, $Ta=25\ C$, $ZO=50\ ohm$ (*)

[Graphs showing gain, return loss, isolation, noise figure, P-1dB, and OIP3 versus frequency.]
ASSEMBLY DIAGRAM:  For use with on-chip match option

Notes:
1) R1=2.5k ohm series resistor is recommended on VG bias line for DC bias isolation.
2) VDD bias choke S1 is 6.5 turn MIC spiral on 10 mil thick alumina substrate. W=1mil, S=1mil, and Outside diameter = 35mil.
3) Please contact factory sales for additional information on external components and matching for improved performance.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETERS</th>
<th>UNITS</th>
<th>MAX</th>
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<tr>
<td>VDD</td>
<td>Drain Voltage</td>
<td>V</td>
<td>6</td>
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<tr>
<td>IDD</td>
<td>Drain Current</td>
<td>mA</td>
<td>150</td>
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<td>Pdiss</td>
<td>DC Power Dissipation</td>
<td>W</td>
<td>0.6</td>
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<tr>
<td>Pn max</td>
<td>RF Input Power</td>
<td>dBm</td>
<td>+17</td>
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<td>Toper</td>
<td>Operating Case/Lead Temp Range</td>
<td>ºC</td>
<td>-40 to +85</td>
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<tr>
<td>Tch</td>
<td>Channel Temperature</td>
<td>ºC</td>
<td>150</td>
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<tr>
<td>Tstg</td>
<td>Storage Temperature</td>
<td>ºC</td>
<td>-60 to 150</td>
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</table>

Exceeding any of these limits may cause permanent damage.
MECHANICAL INFORMATION

Outline Drawing

Notes:
1) Die Size: 1.57 x 0.91 x 0.1 mm
2) Bond Pad Sizes are shown in the above Chip Layout
3) Bond Pad & Backside metallization: Gold
4) All Pads labeled GND1 to GND4 must be bonded to backside GND paddle for DC & RF Grounding with 2 to 3 short 1mil dia wires on each pad.
5) FB1 & FB2 pads may be used to add external larger feedback capacitor in parallel to extend low-frequency range. Additionally low-frequency performance can be extended down to 50 MHz by using a larger external drain bias choke ( > 150 nH)
6) RFIN2 pad may be used to bypass on-chip input inductor & cap to connect external match for reduced noise figure.
7) External Bias choke & Bypass caps on VDD and DC blocking caps on RFIN1/RFOUT1 are required.
8) Please contact factory sales for additional information on external tuning for improved performance.

Functional Diagram