MwT-LN240

26 GHz Super Low Noise pHEMT Device

FEATURES

- **0.5 dB Minimum Noise Figure at 12 GHz**
- **10 dB Associated Gain at 12 GHz**
- **16 dBm P1dB at 12 GHz**
- **0.15 Micron x 240 Micron Gate**

APPLICATIONS

- **Excellent Choice for Super Low Noise Applications**
- **Ideal for Commercial, Military, Hi-Rel Space Applications**

DESCRIPTION

The MwT- LN240 is a super low noise, quasi-enhancement-mode pHEMT whose nominal 0.15 micron gate length and 240 micron gate width makes it ideally suited for applications requiring very low noise figure and high associated gain up to 30 GHz. The device is equally effective for wideband (e.g. 6 to 18 GHz) and narrow-band applications. Each wafer can be screened to meet high quality and reliability requirements for military and space applications.

RF SPECIFICATIONS AT Ta = 25 C

SYMBOL	PARAMETERS & CONDITIONS	FREQ	UNITS	MIN	TYP	MAX
NF min	Minimum Noise Figure Vds=2.5V Ids = 20 mA (Vgs=0)	4 GHz 12 GHz	dB		0.2 0.5	
SSG	Associated Gain Vds=2.5V Ids = 20 mA (Vgs=0)	4 GHz 12 GHz	dB		13 10	
P1dB	Output Power at 1dB Compression Vds=3.0V Ids = 50 mA	12 GHz	dBm		16.0	

Note: MWT-LN240 is a quasi enhancement mode device. For best noise figure, Vgs bias voltage should be set at either 0 or slightly positive voltages to achieve the target operating current.

DC SPECIFICATIONS AT Ta = 25 C

SYMBOL	PARAMETERS & CONDITIONS	FREQ	UNITS	MIN	TYP	MAX
Imax	Saturated Drain Current Vds = 2.5V Vgs = 0.6V		mA		110	
Gm	Transconductance Vds = 2.5V Vgs = 0.2V		mS	140	180	
Vp	Pinch-off Voltage Vds = 2.0V Ids = 0.5mA		V		-0.2	
BVGSO	Gate-to-Source Breakdown Voltage Igs = -0.3mA		V	-6.0	-8.0	
BVGDO	Gate-to-Drain Breakdown Voltage Igd = -0.3mA		V	-7.5	-9.0	
Rth *	Chip Thermal Resistance		ºC/W		300	

* Overall Rth depends on chip mounting

4268 Solar Way
Fremont, CA 94538
sales@mwtinc.com

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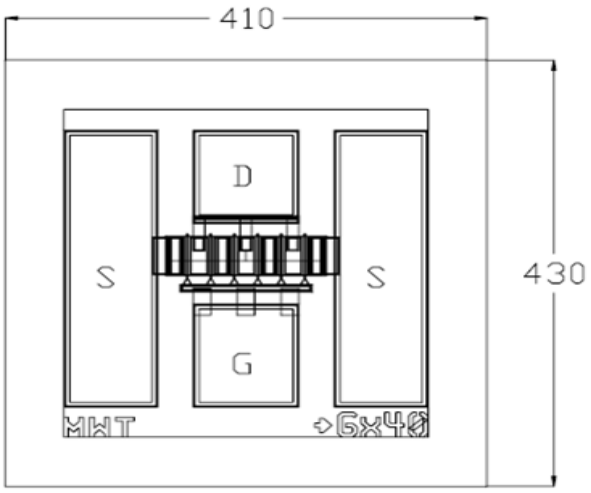
NOISE PARAMETERS Vds=2.5V, Ids=20mA

Freq (GHz)	NFmin (dB)	GA (dB)	Gamma Opt		Rn/50
			Mag	Ang	
2	0.17	16.7	0.826	-6.4	0.14
4	0.20	13.3	0.826	14.4	0.15
6	0.25	11.3	0.81	33.3	0.15
8	0.34	10.5	0.78	50.5	0.14
10	0.42	10.0	0.741	66	0.13
12	0.51	9.7	0.697	79.9	0.12
14	0.59	9.5	0.652	92.3	0.11
16	0.67	9.3	0.609	103.3	0.1
18	0.76	9.0	0.574	113	0.09
20	0.84	8.6	0.551	121.3	0.09
22	0.93	8.0	0.542	128.6	0.09
24	1.01	7.5	0.552	134.7	0.08
26	1.09	7.0	0.586	139.8	0.08

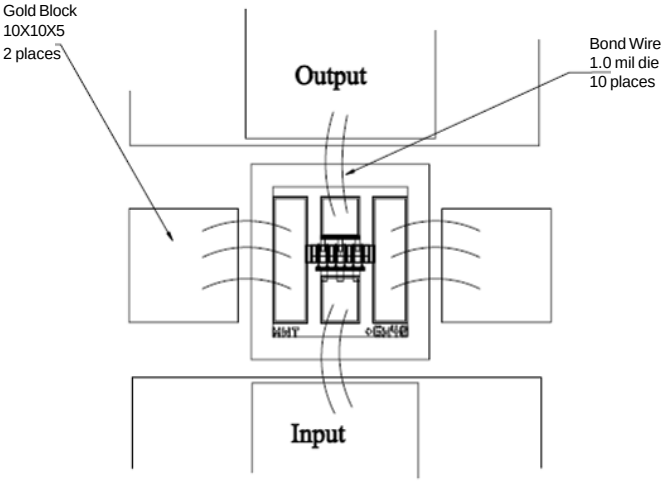


Chip Dimensions: 410 x 430 microns
Source pad: 80 x 280
Gate and Drain pad: 90 x 90
Chip Thickness: 100 microns

S-PARAMETERS V=2.5V, Ids=20mA

F	S11		S21		S12		S22		K	GMAX
GHz	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang		dB
1	0.92	-21.6	9.81	156.1	0.026	74.1	0.50	-18.6	0.35	25.7
2	0.93	-43.4	9.65	151.0	0.050	65.4	0.49	-38.6	0.13	22.9
3	0.90	-61.5	8.79	141.0	0.068	54.2	0.47	-55.7	0.14	21.1
4	0.88	-76.8	7.94	132.1	0.081	46.7	0.46	-69.4	0.13	19.9
5	0.86	-90.2	7.12	124.5	0.093	40.3	0.44	-81.8	0.14	18.8
6	0.85	-100.4	6.42	118.3	0.101	34.5	0.43	-91.4	0.15	18.0
7	0.84	-109.5	5.83	112.7	0.107	29.6	0.43	-99.7	0.16	17.4
8	0.83	-117.5	5.31	107.8	0.111	25.7	0.42	-106.9	0.17	16.8
9	0.83	-124.0	4.86	103.4	0.115	21.7	0.42	-112.8	0.16	16.3
10	0.82	-129.7	4.46	99.5	0.116	18.7	0.41	-118.4	0.19	15.8
11	0.81	-134.4	4.11	96.0	0.118	15.4	0.41	-122.3	0.22	15.4
12	0.80	-138.4	3.82	92.9	0.119	13.6	0.41	-125.4	0.24	15.1
13	0.80	-142.3	3.55	89.8	0.122	11.2	0.41	-128.4	0.24	14.7
14	0.79	-145.5	3.33	87.0	0.122	9.0	0.41	-131.6	0.27	14.4
15	0.80	-148.8	3.12	84.1	0.123	6.7	0.41	-134.4	0.27	14.0
16	0.80	-151.9	2.93	81.6	0.120	5.0	0.41	-137.1	0.28	13.9
17	0.79	-154.2	2.76	79.0	0.123	4.5	0.41	-138.7	0.33	13.5
18	0.78	-157.1	2.62	76.9	0.124	0.9	0.41	-140.9	0.35	13.2
19	0.77	-158.9	2.48	74.5	0.122	1.2	0.41	-142.8	0.40	13.1
20	0.78	-160.6	2.35	72.2	0.122	-0.7	0.40	-143.8	0.41	12.9
21	0.78	-162.3	2.24	70.4	0.121	-2.9	0.40	-143.9	0.43	12.7
22	0.77	-164.3	2.13	68.0	0.118	-3.5	0.40	-146.3	0.51	12.6
23	0.77	-164.9	2.03	66.7	0.120	-4.2	0.41	-146.9	0.50	12.3
24	0.78	-165.7	1.95	64.9	0.120	-5.1	0.42	-148.3	0.50	12.1
25	0.77	-168.5	1.87	63.1	0.118	-5.7	0.41	-149.3	0.56	12.0
26	0.77	-169.6	1.79	61.3	0.114	-7.5	0.41	-148.9	0.63	11.9

RECOMMENDED ASSEMBLY CONFIGURATION



Note: The gold blocks and circuits should be placed as close to the device as possible. The bond wire should be as short as possible.

MAXIMUM RATINGS at Ta = 25 C

Symbol	Parameters	Units	Cont Max 1	Absolute Max 2
VDS	Drain to Source Voltage	V	4.0	4.5
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +160	+180
Pin	RF Input Power	mW	16	30
Pt	Total Power Dissipation	mW	300	400

Exceeding any on of these limits in continuous operation may reduce the mean-time-to-failure below the design goal and may cause permanent damage

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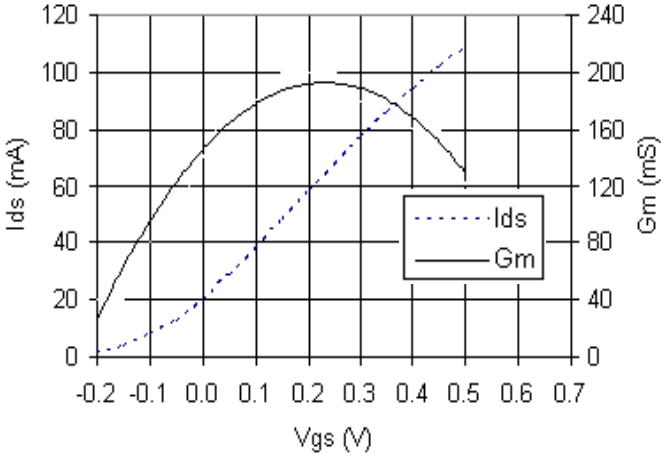
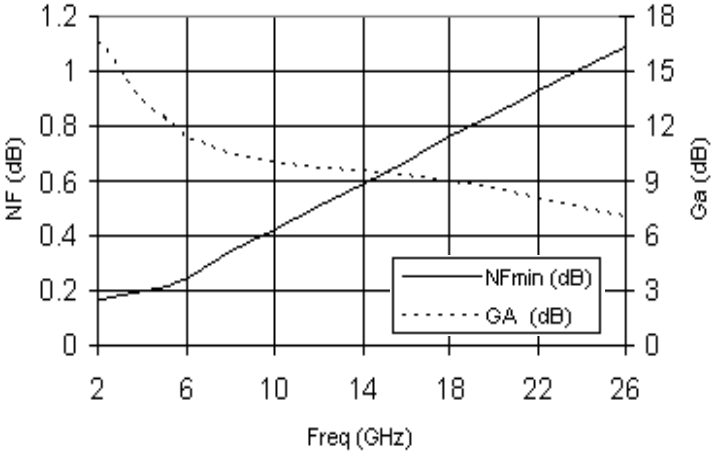
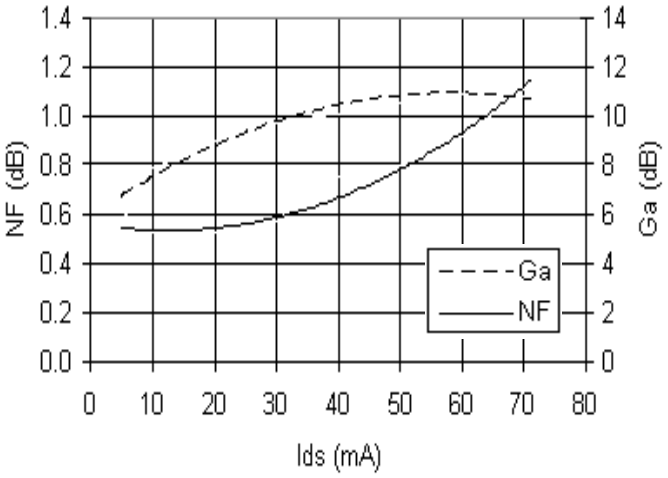
Gm & Ids vs. Vgs
Vds = 2.5V



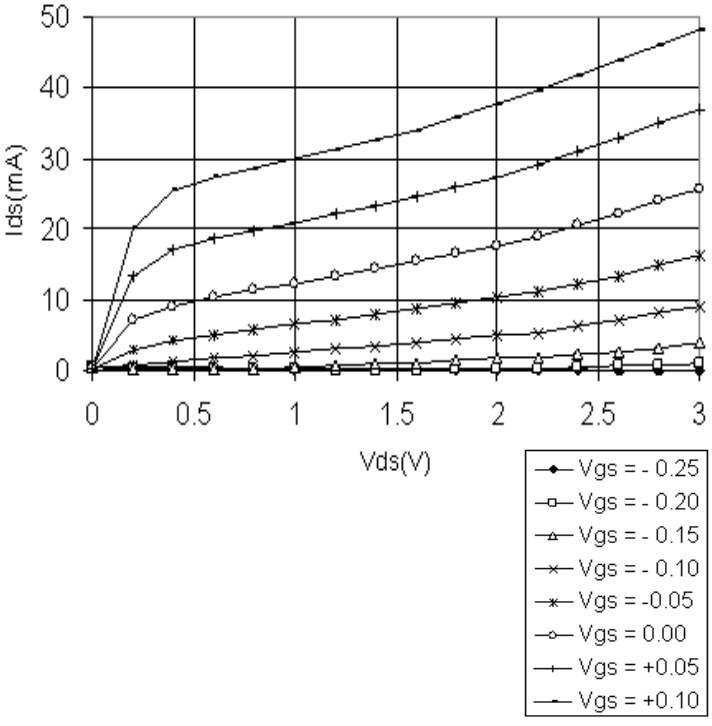
NF & Ga vs. Freq
Vds = 2.5V, Ids = 20mA



NF & Ga vs. Ids
Freq = 12GHz, Vds = 2.5V



DC IV Characteristics



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