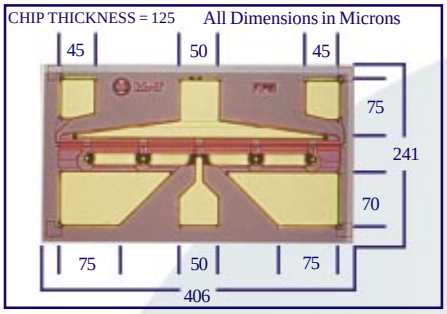
MwT-5

26 GHz High Gain, Dual Gate GaAs FET

DOWNLOAD ADDITIONAL DATA WWW.MWTINC.COM



FEATURES

- 10.5 dB GAIN IN A 6-18 GHz BALANCED CIRCUIT
- +14 dBm P1dB IN A 6-18 GHz BALANCED CIRCUIT
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- HIGH POWER ADDED EFFICIENCY
- DIAMOND-LIKE CARBON (DLC) PASSIVATION
- 2 x 300 MICRON GATE WIDTH

DESCRIPTION

The MwT-5 is a dual gate GaAs MESFET device whose nominal quarter-micron gate length and 300 micron gate width make it ideally suited to applications requiring high-gain in the 500 MHz to 26 GHz frequency range. The straigth gate geometry of the MwT-5 makes it equally effective for either wideband (e.g. 2 to 26 GHz) or narrow-band applications. The chip is produced using MwT's reliable metal system and devices from each wafer are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability, Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

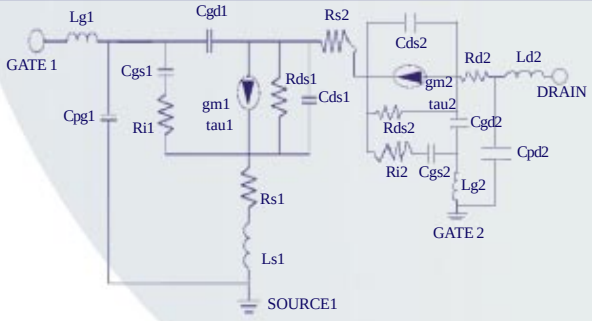
DC SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAM. & CONDITIONS	UNITS	MIN	TYP	MAX
IDSS	Saturated Drain Current Vds= 4.0 V VG1S=VG2S=0.0 V	mA	30		110
Gm	Transconductance Vds= 2.0 V VG2S=0.0 V	mS	23	40	
Vp	Pinch-off Voltage Vds= 3.0 V VG2S=0V IDS=0mA	V		-2.0	-4.5
BVGSO	Gate-to-Source Breakdown Volt. Igs= -0.4 mA	V	-5.0	-8.0	
BVGDO	Gate-to-Drain Breakdown Volt. Igd= -0.4 mA	V	-7.0	-10.0	
Rth	Thermal Resistance MwT-5 Chip *Overall Rth depends on case mounting.	°C/W			150

RF SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1 dB Compression VDS= 6.0 V IDS=0.5xIDSS	6-18 Bal. 12 GHz	dBm	15.0 15.0	18.0 18.0
SSG	Small Signal Gain VDS= 6.0 V IDS=0.5xIDSS	6-18 Bal. 12 GHz	dB	10.0 12.0	10.5 13.0
NF Opt	Optimum Noise Figure VDS= 6.0 V IDS=30 mA	6-18 Bal. 12 GHz	dB		6.0 3.5
GA	Gain@Opt. NF VDS= 6.0V IDS= 30 mA	12 GHz	dB		11
IDSS	Recommended IDSS Range for Optimum P1dB		mA		55-90

DEVICE EQUIVALENT CIRCUIT MODEL



PARAMETER (1)		VALUE	
Source Resistance	Rs	0.7	Ω
Source Inductance	Ls	0.04	nH
Drain-Source Resistance	Rds	100	Ω
Drain Pad Capacitance	Cpd	0.01	pF
Gate Bond Wire Inductance	Lg	0.173	nH
Gate Pad Capacitance	Cpg	0.01	pF
Gate-Source Capacitance	Cgs	0.159	pF
Channel Resistance	Ri	4.37	Ω
Gate-Drain Capacitance	Cgd	0.105	pF
Transconductance	gm	44.0	mS
Transit Time	tau	2.0	psec

PARAMETER (2)		VALUE	
Gate Bond Wire Inductance	Lg	0.12	nH
Gate-Source Capacitance	Cgs	0.166	pF
Channel Resistance	Ri	5.7	Ω
Gate-Drain Capacitance	Cgd	0.056	pF
Transconductance	gm	52.0	mS
Transit Time	tau	2.0	psec
Source Resistance	Rs	3.0	Ω
Drain-Source Resistance	Rds	205	Ω
Drain-Source Capacitance	Cds	0.01	pF
Drain Resistance	Rds	4.3	Ω
Drain Bond Wire Inductance	Ld	0.253	nH
Drain Pad Capacitance	pF	0.01	pF

ORDERING INFORMATION

Chip MwT-5

NOTE:
For Package information, please see supplimentary application note from our website at www.mwtinc.com. When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

4268 Solar Way Fremont California 94538 Phone: (510) 651-6700 Fax: (510) 651-2208

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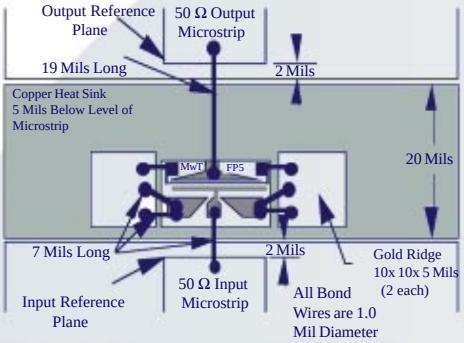
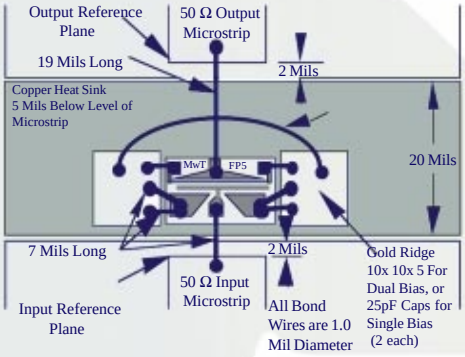
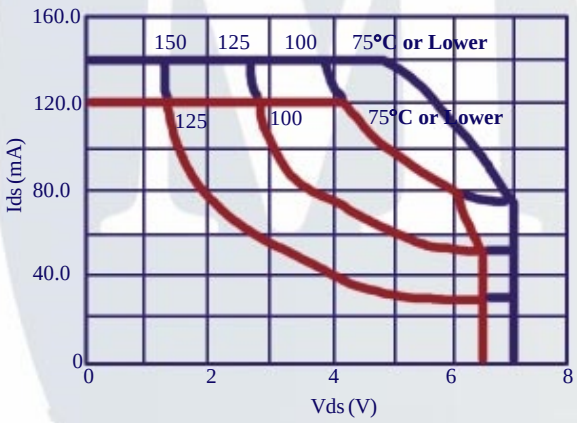
DUAL BIAS



MwT-5
OPTIONAL BONDING



SAFE OPERATING LIMITS vs. BACKSIDE CHIP



Absolute Maximum Continuous Maximum

MAXIMUM RATINGS AT Ta = 25°C

SYMBOL	PARAMETER	UNITS	CONT MAX[1]	ABSOLUTE MAX[2]
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	95	145

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

Bin	A	B	C	D
Idss Range	30-40	40-55	55-85	85-100

BIN ACCURACY STATEMENT

When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

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