MicroWave Technology
An IXYS Company

MwT-LN180

26 GHz Super Low Noise pHEMT Device
May 2010

FEATURES

- **0.5 dB Minimum Noise Figure at 12 GHz**
- **10 dB Associated Gain at 12 GHz**
- **16.0 dBm P1dB at 12 GHz**
- **0.15 Micron x 180 Micron Gate**

APPLICATIONS

- **Excellent Choice for Super Low Noise Applications**
- **Ideal for Commercial, Military, Hi-Rel Space Applications**

DESCRIPTION

The MwT- LN180 is a super low noise, quasi-enhancement-mode pHEMT whose nominal 0.15 micron gate length and 180 micron gate width makes it ideally suited for applications requiring very low noise applications up to 30 GHz frequency. The device is equally effective for wideband (e.g. 6 to 18 GHz) and narrow-band applications. Each wafer can be screened to meet the high quality and reliability requirements for military and space applications.

RF SPECIFICATIONS AT Ta = 25 C

SYMBOL	PARAMETERS & CONDITIONS	FREQ	UNITS	MIN	TYP	MAX
NF min	Minimum Noise Figure Vds=2.5V Ids = 14 mA (Vgs=0)	4 GHz 12 GHz	dB		0.2 0.5	
SSG	Associated Gain Vds=2.5 V Ids = 14 mA (Vgs=0)	4 GHz 12 GHz	dB		14.5 10.0	
P1dB	Output Power at 1dB Compression Vds=3.0 V Ids = 50 mA	12 GHz	dBm		16.0	

Note: MWT-LN180 is a quasi enhancement mode device. For best noise figure, Vgs bias voltage should be set at either 0 or slightly positive voltages to achieve the target operating current.

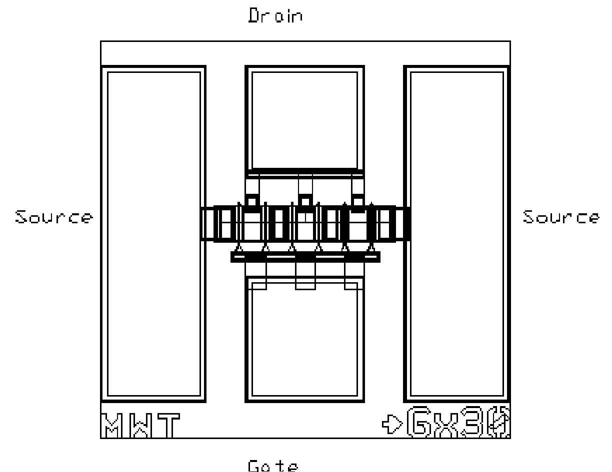
DC SPECIFICATIONS AT Ta = 25 C

SYMBOL	PARAMETERS & CONDITIONS	FREQ	UNITS	MIN	TYP	MAX
Imax	Saturated Drain Current Vds = 2.5V Vgs = 0.6V		mA		70	
Gm	Transconductance Vds = 2.5V Vgs = 0.2V		mS	140	180	
Vp	Pinch-off Voltage Vds = 2.0V Ids = 0.5mA		V		-0.2	
BVGSO	Gate-to-Source Breakdown Voltage Igs = -0.3mA		V	-6.0	-8.0	
BVGDO	Gate-to-Drain Breakdown Voltage Igd = -0.3mA		V	-7.5	-9.0	
Rth *	Chip Thermal Resistance		^{0}C/W		300	

* Overall Rth depends on chip mounting

NOISE PARAMETERS Vds=2.5V, Ids=14mA

Freq (GHz)	NFmin (dB)	GA (dB)	Gamma Opt Mag	Gamma Opt Ang	Rn/50
2	0.17	18	0.73	-3.7	0.17
4	0.20	15	0.806	11.6	0.18
6	0.26	11.8	0.841	26.4	0.19
8	0.35	10.5	0.841	40.8	0.18
10	0.43	10	0.815	54.4	0.17
12	0.52	10	0.769	67.2	0.16
14	0.61	10	0.712	0.79.1	0.15
16	0.69	9.8	0.652	89.9	0.14
18	0.78	9.5	0.595	99.5	0.13
20	0.86	9.1	0.549	107.8	0.12
22	0.95	8.5	0.523	114.6	0.12
24	1.03	8	0.523	119.8	0.12
26	1.12	7.2	0.558	123.3	0.13

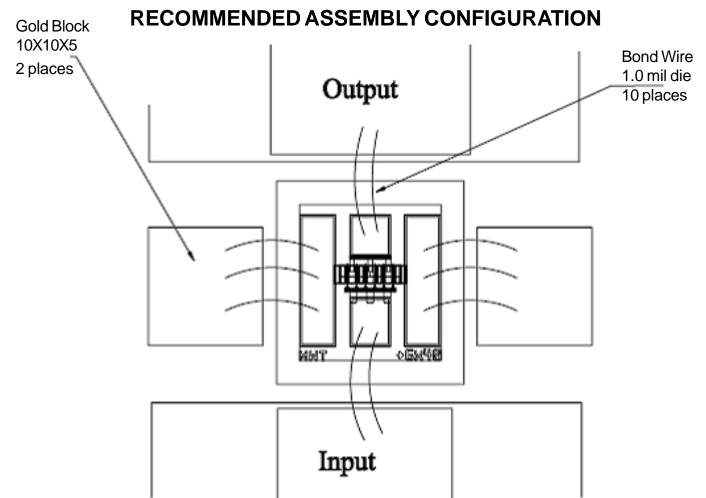


Chip Dimensions: 410 x 430 microns
Source pad: 80 x 280
Gate and Drain pad: 90 x 90
Chip Thickness: 100 microns

S-PARAMETERS V=2.5V, Ids=14mA

F [GHz]	S11 Mag	S11 Ang	S21 Mag	S21 Ang	S12 Mag	S12 Ang	S22 Mag	S22 Ang	K	GMAX dB
1	0.97	-16.8	8.44	165.9	0.024	77.2	0.58	-11.8	0.20	25.5
2	0.95	-32.7	8.06	157.2	0.046	70.8	0.57	-26.2	0.11	22.4
3	0.93	-47.3	7.59	148.5	0.066	61.6	0.55	-38.8	0.12	20.6
4	0.91	-60.4	7.08	140.4	0.082	55.0	0.54	-50.0	0.11	19.4
5	0.89	-72.5	6.55	133.1	0.095	48.1	0.51	-60.5	0.11	18.4
6	0.87	-82.5	6.06	126.9	0.105	42.2	0.50	-69.0	0.13	17.6
7	0.86	-91.7	5.60	121.1	0.114	37.2	0.48	-77.1	0.13	16.9
8	0.85	-100.1	5.20	115.8	0.122	32.7	0.47	-84.3	0.14	16.3
9	0.84	-107.0	4.83	111.1	0.126	29.0	0.46	-90.3	0.14	15.8
10	0.83	-113.4	4.48	106.8	0.130	25.2	0.45	-96.3	0.16	15.4
11	0.82	-118.8	4.17	102.9	0.134	22.0	0.43	-100.8	0.18	14.9
12	0.80	-123.3	3.90	99.5	0.136	19.2	0.43	-104.9	0.21	14.6
13	0.80	-127.7	3.65	96.0	0.137	16.4	0.42	-108.6	0.21	14.2
14	0.79	-131.5	3.44	93.0	0.141	14.1	0.42	-112.5	0.23	13.9
15	0.80	-135.6	3.24	89.9	0.142	11.9	0.42	-116.0	0.23	13.6
16	0.79	-139.1	3.06	87.1	0.141	8.5	0.42	-118.8	0.24	13.4
17	0.79	-141.9	2.89	84.3	0.140	7.7	0.41	-121.5	0.27	13.2
18	0.77	-145.0	2.74	81.9	0.141	5.6	0.41	-123.6	0.32	12.9
19	0.77	-147.8	2.60	79.3	0.142	3.8	0.41	-126.1	0.33	12.6
20	0.78	-149.7	2.47	77.0	0.145	3.2	0.40	-128.4	0.34	12.3
21	0.77	-151.8	2.36	74.9	0.143	-0.6	0.40	-129.4	0.37	12.2
22	0.76	-153.8	2.25	72.4	0.144	-1.7	0.40	-131.2	0.41	12.0
23	0.76	-155.5	2.15	70.7	0.142	-2.5	0.40	-132.4	0.42	11.8
24	0.76	-156.5	2.07	68.8	0.139	-4.9	0.40	-134.2	0.44	11.7
25	0.75	-159.8	1.97	66.8	0.140	-7.2	0.40	-135.4	0.51	11.5
26	0.75	-160.6	1.90	64.9	0.146	-5.9	0.40	-136.2	0.51	11.1

RECOMMENDED ASSEMBLY CONFIGURATION



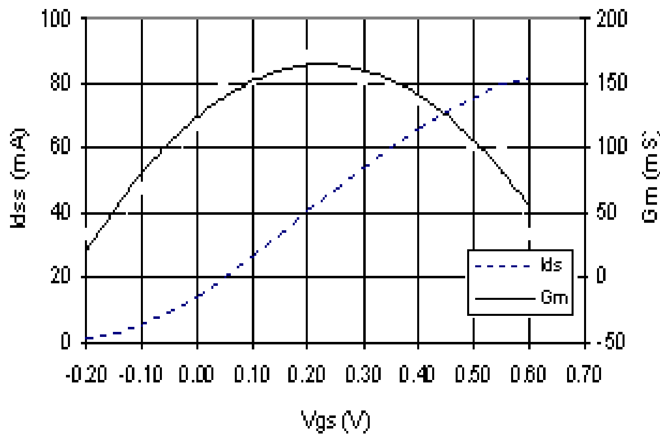
Note: The gold blocks and circuits should be placed as close to the device as possible. The bond wire should be as short as possible.

MAXIMUM RATINGS at Ta = 25 C

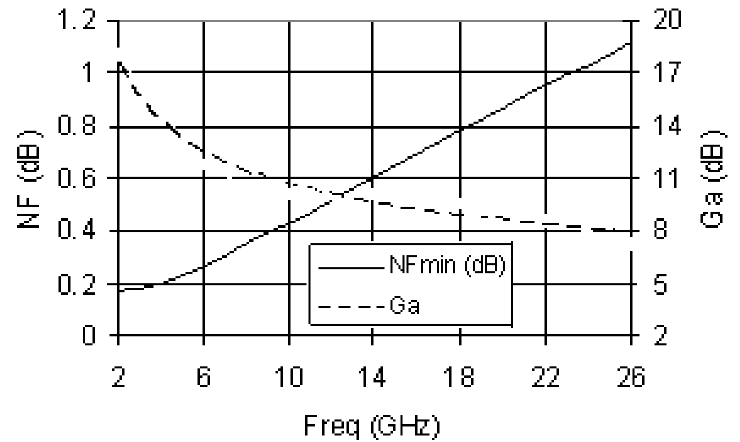
Symbol	Parameters	Units	Cont Max 1	Absolute Max 2
VDS	Drain to Source Voltage	V	4.0	4.5
Tch	Channel Temperature	ºC	+150	+175
Tst	Storage Temperature	ºC	-65 to +160	+180
Pin	RF Input Pow er	mW	10	20
Pt	Total Pow er Dissipation	mW	100	150

Exceeding any on of these limits in continuous operation may reduce the mean-time-to-failure below the design goal and may cause permanent damage

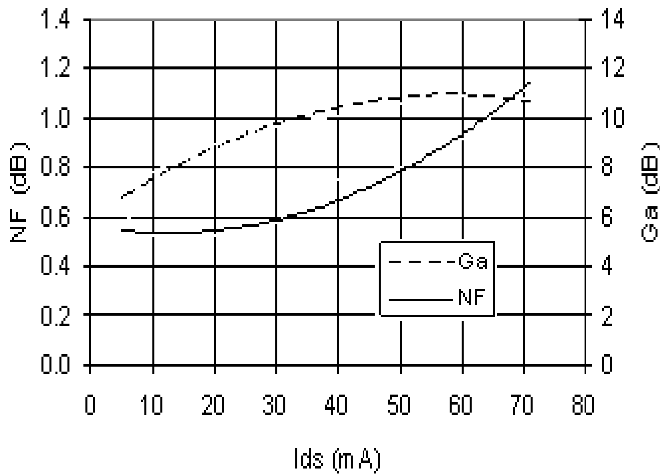
Gm & Ids vs. Vgs
Vds = 2.5V



NF & Associated Gain vs. Freq
Vds = 2.5V, Ids = 14mA



NF & Ga vs. Ids
Freq = 12GHz, Vds = 2.5V



DC IV Characteristics