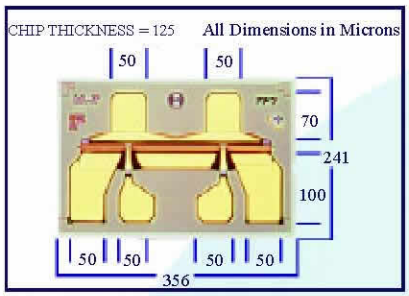
MwT-LP7

Ultra - Low Phase Noise device up to 31 GHz

DOWNLOAD ADDITIONAL DATA WWW.MWTINC.COM



FEATURES

- Ultra - Low Phase Noise for Oscillator Applications up to 31 GHz
- Also Excellent for Broadband Gain and Medium Power Applications
- +20 dBm Output Power at 12 GHz
- 0.3 Micron Refractory Metal/Gold Gate
- 250 Micron Gate Width
- Choice of Chip and Two Package Types

DESCRIPTION

The MwT-LP7 is a low phase noise GaAs MESFET device with nominal quarter-micron gate length and 250-micron gate width. With deep understanding on the physical origins of phase noise, the device is built by using a unique proprietary technology to minimize the phase noise. This device is particularly attractive to oscillator applications requiring ultra-low phase noise up to 31 GHz or amplifiers requiring low residue noise in the 500 MHz to 26 GHz frequency range. A 17.5 GHz DRO using this device achieved phase noise power density as low as -119 dBc/Hz at 100 kHz off set with ample output power of +15dBm. The device is equally effective for either wideband (e.g. 6 to 18 GHz) or narrow-band applications. The chip is produced using MwT's reliable metal system and all devices from each wafer are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability. Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

DC SPECIFICATIONS AT Ta = 25°C

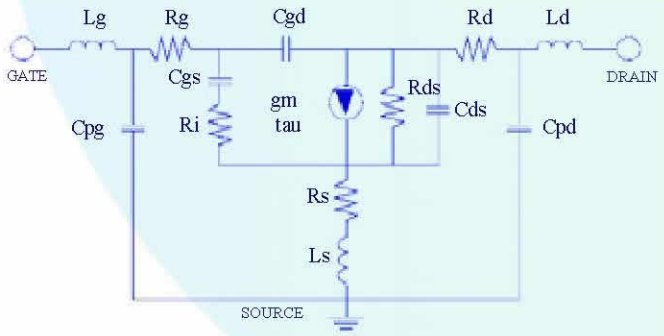
SYMBOL	PARAM. & CONDITIONS	UNITS	MIN	TYP	MAX
IDSS	Saturated Drain Current Vds= 3.0 V VGS= 0.0 V	mA	38		98
Gm	Transconductance Vds= 3.0 V VGS= 0.0 V	mS	36	45	
Vp	Pinch-off Voltage Vds= 3.0 V IDS= 1.0 mA	V		-1.5	-4.5
BVGSO	Gate-to-Source Breakdown Volt. Igs= 0.4 mA	V	-5.0	-8.0	
BVGDO	Gate-to-Drain Breakdown Volt. Igd= 0.4 mA	V	-6.0	-8.0	
Rth	Thermal Resistance MwT-LP7 Chip, MwT-LP770, LP773	°C/W			180 380*

*Overall Rth depends on case mounting.

RF SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1 dB Compression VDS= 5.0 V Idss= 0.6 IDS=40mA	12 GHz	dBm	18.0	20.0
SSG	Small Signal Gain VDS= 5.0 V Idss= 0.6 IDS=40mA	12 GHz	dB	10.0	11.0
NFopt	Optimum Noise Figure VDS= 3.0V IDS= 15mA	12 GHz	dB		2.0
GA	Gain at Optimum Noise Figure VDS= 3.0V IDS= 15mA	12 GHz	dB		8.0
IDSS	Recommended IDSS Range for Optimum P1dB		mA		50-86

DEVICE EQUIVALENT CIRCUIT MODEL



PARAMETER		VALUE	
Source Resistance	Rs	2.6	Ω
Source Inductance	Ls	0.025	nH
Drain-Source Resistance	Rds	230	Ω
Drain-Source Capacitance	Cds	0.07	pF
Drain Resistance	Rd	3.67	Ω
Drain Pad Capacitance	Cpd	0.027	pF
Drain Inductance	Ld	0.159	nH
Gate Bond Wire Inductance	Lg	0.89	nH
Gate Pad Capacitance	Cpg	0.05	pF
Gate Resistance	Rg	0.2	Ω
Gate-Source Capacitance	Cgs	0.314	pF
Channel Resistance	Ri	6.9	Ω
Gate-Drain Capacitance	Cgd	0.03	pF
Transconductance	gm	55	mS
Transit Time	tau	3.02	psec

ORDERING INFORMATION

Chip	MwT-LP7
Package 70	MwT-LP770
Package 73	MwT-LP773

NOTE:
For Package information, please see supplementary application note from our website at www.mwtinc.com. When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

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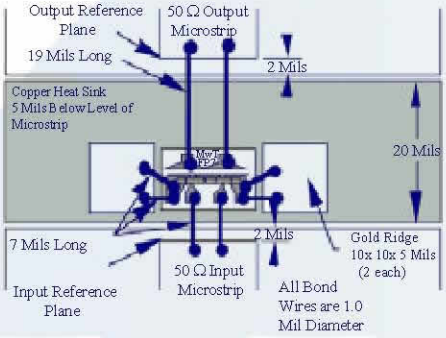
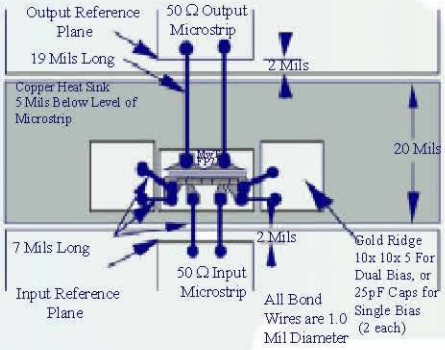
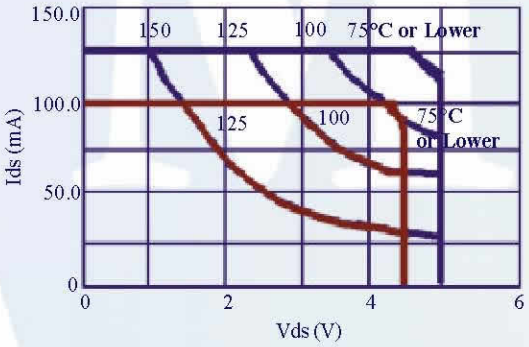
MwT-LP7
DUAL BIAS



MwT-LP7
OPTIONAL BONDING



SAFE OPERATING LIMITS vs. BACKSIDE CHIP



MAXIMUM RATINGS AT Ta = 25°C

SYMBOL	PARAMETER	UNITS	CONT MAX[1]	ABSOLUTE MAX[2]
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	80	120

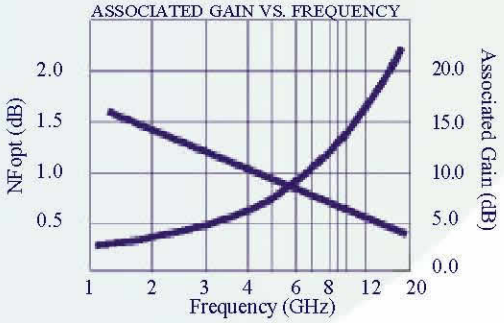
NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

TYPICAL NOISE PARAMETERS

MwT-A9LN Chip: VDS= 3.0V IDS= 35mA

FREQUENCY GHz	NF MIN dB	GAMMA OPT MAG	GAMMA OPT ANGLE	Rn/50
2.00	0.29	0.68	27	0.188
4.00	0.56	0.49	57	0.182
8.00	1.06	0.41	114	0.165
12.00	1.5	0.49	149	0.152
16.00	1.89	0.55	168	0.143
18.00	2.1	0.58	175	0.14

NOISE FIGURE AND
ASSOCIATED GAIN VS. FREQUENCY



Bin Selection Guide

Bin	A	B	C	D
Idss Range	26-38	38-50	50-74	74-86

BIN ACCURACY STATEMENT

When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

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