MMA-005022B

Application note v.1.0
1/17/2011

Introduction

This application note is an operational guide for MwT's MMA005022 Traveling Wave Amplifier (TWA). On-board measurements, utilizing MwT's evaluation module, are illustrated with the design and operational guidelines presented. The evaluation module consists of a laminate printed circuit board design and provides a connectorized environment for ease of evaluation of the device, either individually or with other modules. Since the RF connectors are of a coplanar waveguide design, the PCB has to have either a coplanar or coplanar to microstrip transition design. Measurements presented herein are of a coplanar PCB design, as shown in Figure 1.

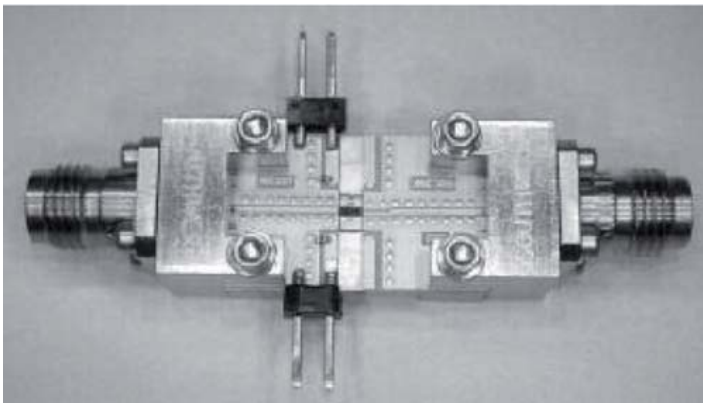

Figure 1. Coplanar PCB Design

Device Description

The MMA005022 is a broadband PHEMT GaAs MMIC designed for medium output power (22.5 dBm P1dB) and high gain (15.5 dB) over a 30 kHz to 50 GHz frequency range. The amplifier is a nine-stage cascode FET structure that ensures flat gain and power as well as uniform group delay. For operation below 2 GHz, additional passive components are necessary to extend the low frequency end of the band down to 30 kHz. With low frequency bias components, the MMA005022 may be used in a variety of time-domain applications through 40 GB/s. The MMA005022 also features a gain control.

Device Operation

The MMA005022 is biased with a single positive drain supply (Vdd) and a negative gate supply (Vg1). For best overall performance, the recommended bias is Vdd = 7 V and Idd = 200 mA. To achieve this drain current level, Vg1 is typically between -2.5 to -3.5 V. Typical DC current flow for Vg1 is -10 mA. The MMA005022 has a second gate bias (Vg2) that may be used for gain control. When not being utilized, Vg2 should be left open circuited. The cascode bias structure of the TWA results in an RF "hot" drain bias that must be isolated from the drain DC supply. This topology creates the need for a decoupling bias network on the drain bias line. Decoupling is the isolation of RF and DC circuits on a common line. The decoupling network is usually a low-pass filter, as shown in Figure 2.

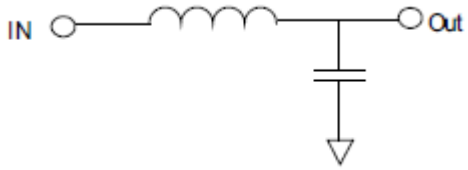

Figure 2. Decoupling Network

The decoupling bias circuit will pass DC to the drain line of the TWA and prevent the RF signal, present on the drain line, from appearing on the DC bias line. This bias network configuration is also referred to as an RF choke. The corner frequency (low frequency roll-off) of the drain bias RF choke is determined by the parallel combination of the drain inductance and the on-chip 50 Ω resistor shown below in Figure 3.

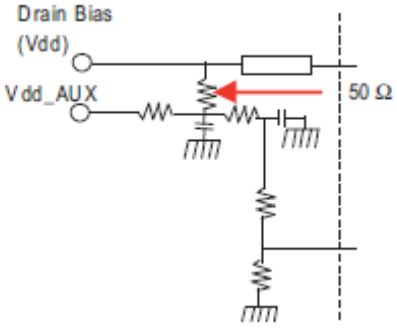

Figure 3. On-chip 50 Ω Resistor

The lower frequency limit (f_{LD}) due to this inductance can be calculated using the following equation.

$$f_{LD} = \frac{Ro}{(2\pi L_D)} \text{ (Hz)}$$

Where, R_O is the RF input/output 50 Ω terminating resistance, and L_D is the inductance associated with the off-chip drain bias circuit. For 2-40GHz operation, the minimum drain inductance is 4.5 nH. A 0.007 in. diameter gold wire with a length of approximately 0.200 in. will achieve this value. Spiral chip inductors are also available with typical dimensions of 0.030 x 0.030 x 0.007 in. It is important to note that capacitive parasitics, in the drain bias network will result in resonances in the frequency response of the TWA. Therefore, it is strongly recommended to reduce parasitic capacitance as much as possible. To minimize resonances, an inductor with a high self-resonate frequency is recommended. If a spiral chip inductor is used, a 50 to 200 Ω, parallel de-queuing resistor will also be necessary. A thin film alumina resistor is recommended for minimal associated parasitics. The schematic in Figure 14 illustrates the external bias recommended for basic operation. Input and output RF ports are DC coupled and will require DC blocking capacitors, C1 and C2, if DC is present on these paths. Selection of DC blocks will be dependent on operating frequency bandwidth. See Table 1 for recommended passive components.
The schematic in Figure 15 illustrates external bias for utilizing the detector and Vg2 gain control.

Low Frequency Extension

As the area required for capacitive bypass lower than 2 GHz would be quite large, the MMA005022 provides the Vdd Auxilary (support) bypass pad, shown in Figure 4, to add the additional large capacitance as required.

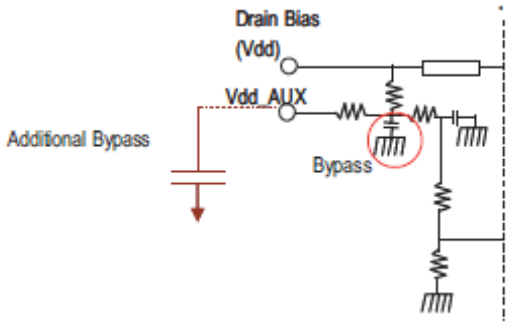

Figure 4. Vdd Auxilary (support) Bypass Pad

The MMA005022 can operate down to frequencies as low as a few hundred kilohertz by:
1) Adding external capacitors to the auxiliary drain pad and Vg1 gate pads.
2) Increasing the capacitance of the DC blocking capacitors at the RF input and output.
3) Increasing the inductance of the drain inductor (L1, Figure 5) to provide high impedance bias feed at the lower frequencies.

All three factors are equally important since any one of these can limit the low frequency performance. Input and output return loss degrades as the drain and gate line loads deviate from 50 Ω. The load can be restored close to 50 Ω and RF performance improved by adding large external capacitors in parallel with the on-chip capacitors, as shown in Figure 5. When the additional bypass capacitors are connected, the low frequency limit is extended down to the corner frequency determined by the bypass capacitors, the combination of the on-chip 50 _ load, and the small de-queing resistor. At this low-end band edge, the small signal gain will increase in magnitude and stay at this elevated level down to the point where the CAUX bypass capacitor acts as an open circuit, effectively rolling off the gain completely. The low frequency capacitive extension limit can be approximated from the following equation:

$$f_{C_{AUX}} = \frac{1}{2\pi (R_o + R_{DE\text{-}Q}) C_{AUX}} \text{ (Hz)}$$

Where, R_O is the 50 Ω gate or drain line terminating resistor. R_{DE} is the small series (<15 Ω de-queing resistor). C_{AUX} is the capacitance of the bypass capacitor connected to the Aux Drain or gate pad, in farads.

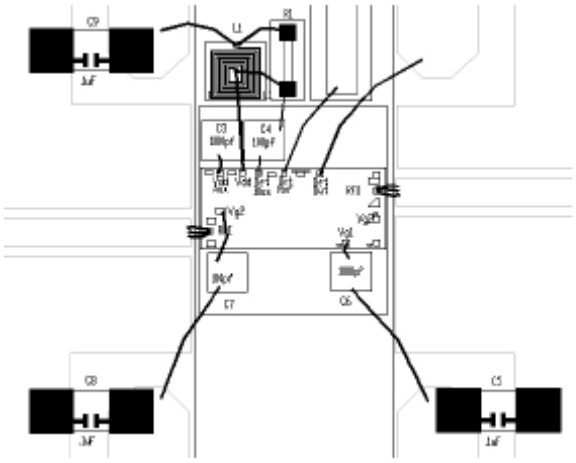

Figure 5

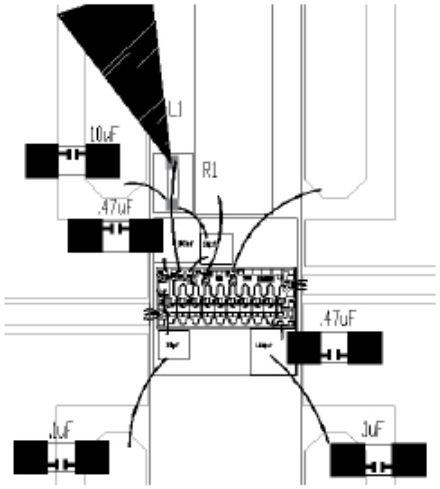

Figure 6

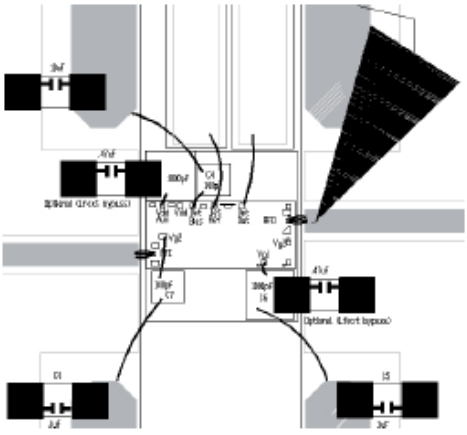

Figure 7

Using this equation, C_{DC} can be calculated for different desired corner frequencies. The equation is an approximation because it does not take into account other factors, such as transmission line impedances and TWA termination networks. In a typical assembly, the bypass capacitors are usually mono-block capacitors on the order of 0.01 or 0.47 µF, depending on the desired low frequency operating point. Keep in mind that these mono-blocks have series parasitic inductance. Since the RF DC blocking capacitors are the most sensitive, in this respect, we show a few recommended broadband DC blocks in Table 1. Figure 5, illustrates a 2 GHz to 50 GHz laminate PCB assembly. L1 is a chip inductor, and R1 is the de-queing alumina chip resistor. Figure 6, illustrates a 10 MHz to 50 GHz laminate PCB assembly. L1 is a Piconics broadband inductor. This inductor has an iron filling that negates the parallel resistor for de-queing. R1 is used simply as a means of launching the inductor and providing bias to the on-chip detector. As discussed previously, as the DC bias is on the same electrical path as the RF path, it is possible to bias the TWA through the RF transmission line. Figure 7 below illustrates this alternative method. The 2 GHz to 40 GHz RF performance, using a 7 turn Micrometrics chip inductor, are illustrated in Figure 8. All module losses are included in this data.

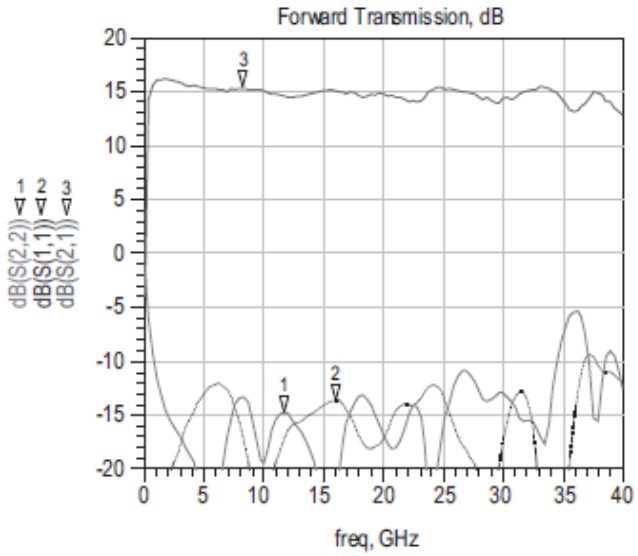

Figure 8. 2 to 40 GHz S-parameters using a seven-turn micrometrics chip inductor

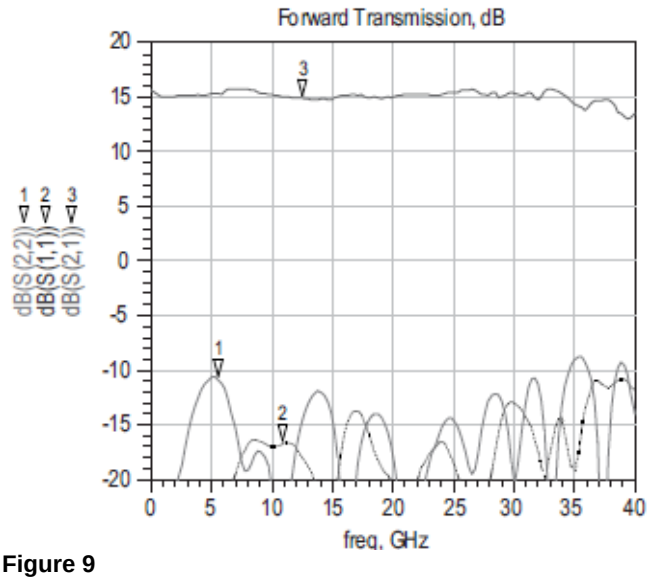

Figure 9

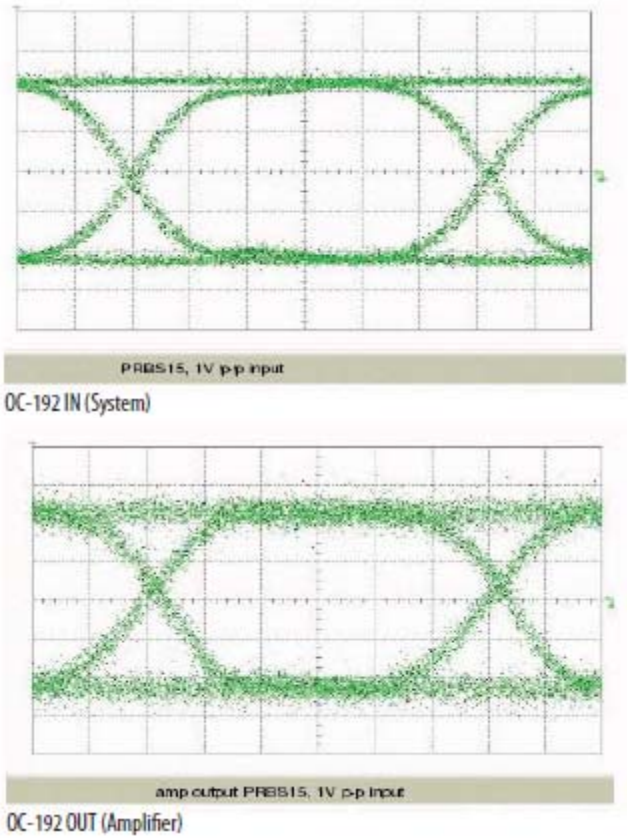

Figure 10. OC-192 Performance

Gain Control Using Vg2

This feature further enhances the versatility of applications where variable gain over a broad bandwidth is necessary. The second gate bias (Vg2) is connected to the gates of the upper FETs in each cascode stage through a small de-queing resistor. The other end of the gate line is terminated in an on-chip resistive/diode divider network, which allows the second gate to self-bias. Thus, with Vg2 left open circuited, the drain current is set by the (Vg1) gate bias voltage applied to the lower FET in each stage. The nominal open circuit voltage for Vg2 is approximately 2 V. Under this operating condition, maximum gain and power are achieved from the TWA. By applying an external voltage to the second gate bias (Vg2) less than the open-circuit potential, the drain voltage on the lower FET can be decreased to a point where the lower FET enters the linear operating region. This reduces the current drawn by each stage. Decreasing Vg2 further will reduce the drain voltage on the lower FET towards zero while pinching off the upper FET in each stage. At larger negative values of Vg2 (between 0 and -2.5 V) the gain of the TWA will decrease significantly. This is illustrated in Figures 11, 12 and 13.

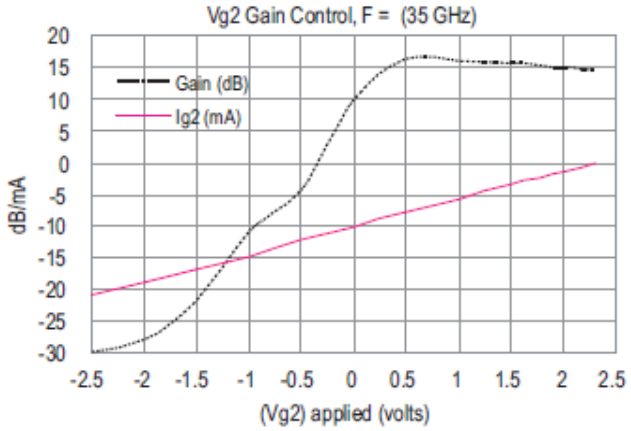

Figure 11. Vg2 vs. Gain @ 35 GHz

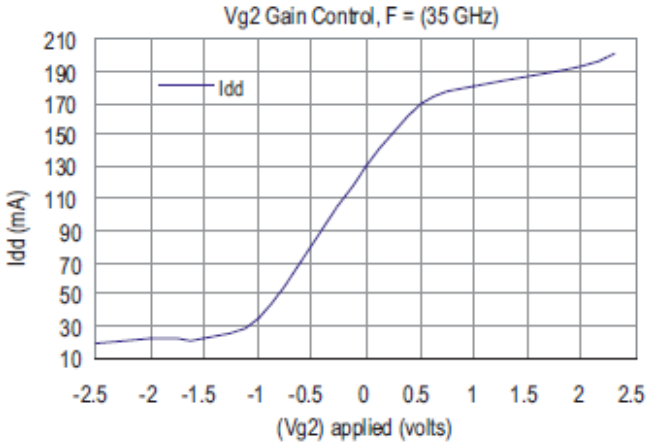

Figure 12. Vg2 vs. Drain Current

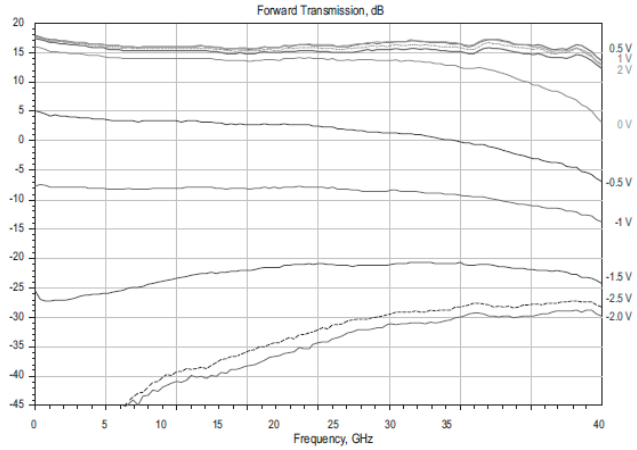

Figure 13. Vg2 Gain Control vs. Frequency

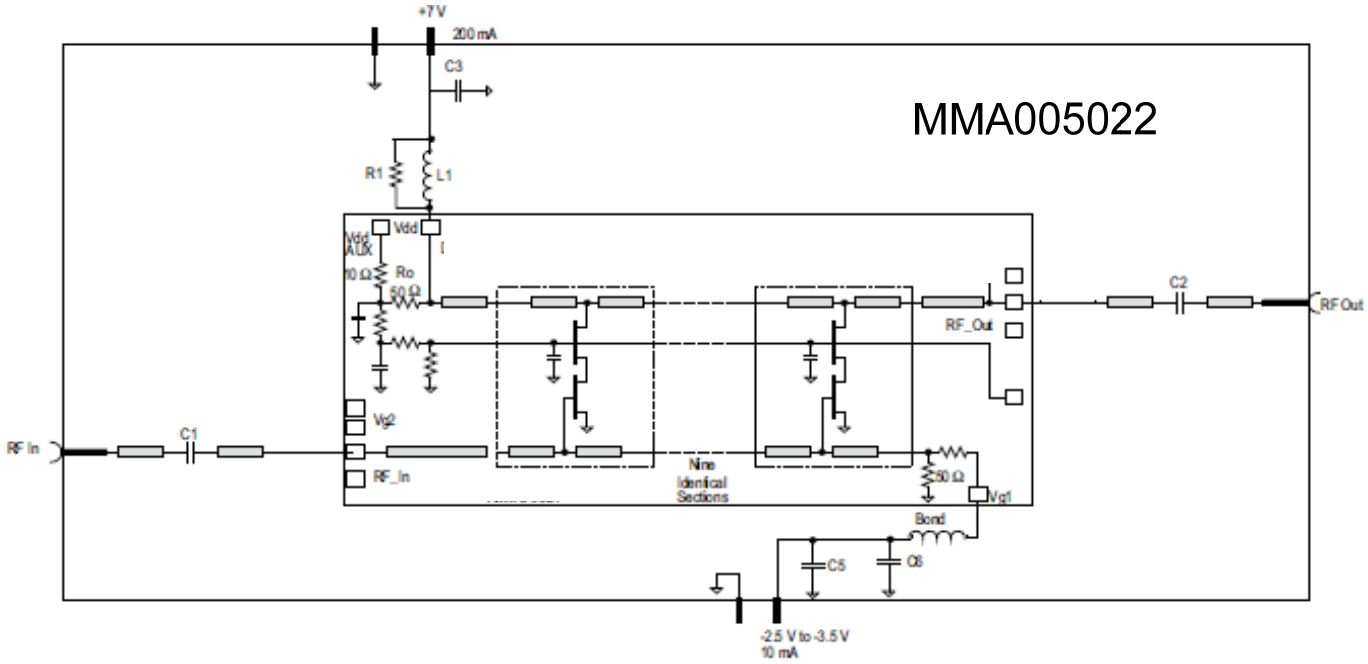

Figure 14. Basic 2 GHz to 40 Ghz Schematic

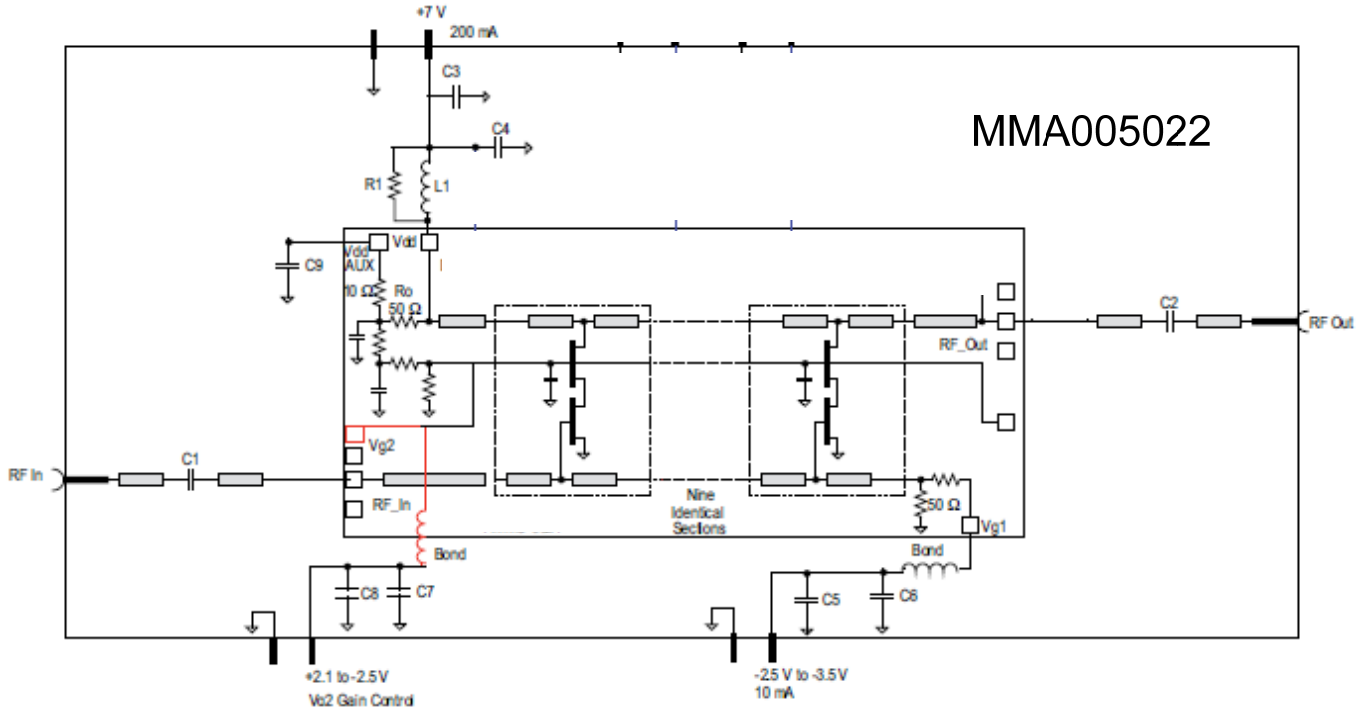

Figure 15. Low Frequency Bypass with a Gain control (Vg2)

Table 1. Recommended Passives for the MMA005022, 30 kHz - 50 GHz TWA

Passive Type	Description	Vendor	Part#	Qty
100 pf Capacitor	Bypass Cap	Presidio	SA1515BX101M2HX5#00XF	4
0.1 µF Capacitor	Bypass Cap	AVX	AVX0402YG104ZAT2A	3
1000 pf Capacitor	Vdd Aux/Vg1 Bypass	Tecdia	SK04B102M11A6	2
0.47 µF Capacitor	Vdd Aux Bypass Cap	Murata	GRP155F51A474ZDO2B	1
*BB DC block capacitors	DC Block Cap	Presidio	BB0302X7R123M16VP8205	2
*BB DC block capacitors	DC Block Cap	ATC	545L Series	2
10 MHz-40 GHz Inductor	BB RF Choke	Piconics	CC45T47K240G5C2	1
*Spiral chip Inductor	Selective RF Choke	MicroFab	www.microfabnh.com	1
*Spiral chip Inductor	Selective RF Choke	Micrometrics	www.micrometrics.com	1
**Alumina Chip Resistor	De-queing Resistor	ATP	www.thinfilm.com	1

*You may use either vendor for these passives
**ATP is a custom thin film substrate manufacturer. Substrate material should be alumina and may be unpolished.

Module Assembly

The most important factor in any microcircuit assembly is choosing materials that are well matched in their physical properties and rated highest for thermal transfer properties. It is also critical that components and materials be evaluated to determine frequency bandwidth limitations. MwT's evaluation modules are assembled in a series of temperature steps that allow re-work, if necessary. A copper-tungsten heat sink that has been nickel/gold plated serves as the base of the assembly. Assembly begins with the attachment of a nickel/gold plated molybdenum pedestal to the base heat sink with Gold/Germanium (Au/Ge) at 300ºC. The pedestal is a good physical match with the IC and is used to ensure that the device is as flush as possible with the surface of the PCBs, thus reducing bond wire lengths and their associated inductance, which can degrade performance above 20 GHz. Close alignment of the PCB RF transmission lines to the IC input and output ports also help minimize bond wire lengths. The stack-up is illustrated in Figure 16. The printed circuit boards are designed on Rogers RO4003 (0.008" thick) material that has a dielectric constant of 3.38. The RO4003 material has low loss up to 50 GHz and is durable enough to withstand thermosonic or thermocompression gold wire bonding as well as soldering of SMT passive components.

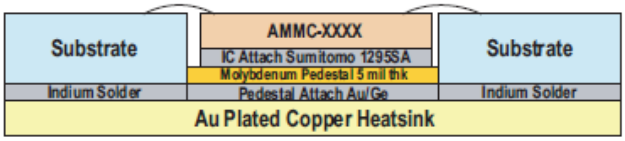

Figure 16. PCB Detail

Summary

In summary, this application note has given operational guidance for utilizing the MMA005022 TWA's broad 30 kHz to 50 GHz bandwidth. This note has also shown examples of performance for designs discussed in this note and illustrated details of the evaluation module assembly used to measure the TWA design configurations. It is important to keep in mind that the cascode bias structure of the TWA results in an RF "hot" drain bias that must be isolated from the drain DC supply, and the decoupling network designed to separate the two circuits should be designed with as minimal parasitic capacitance as possible. Also, it is critical to minimize series parasitic inductance in the RF path. This includes bond wire lengths as well as associated parasitic inductance in the DC blocking capacitors.

Reference

Volkan Kaman, Tom Reynolds, Anders Petersen, and John E. Bowers "A 100KHz to 50GHz Travelling-Wave Amplifier IC Module", IEEE Microwave and Guided Wave Letters, Vol. 9, No. 10, October 1