## **FET Application Notes**

**Supplimentary Information** 



## **Device Handling Procedure**

- 1) Open package in clean room environment only.
- 2) GaAs FETs are sensitive to electrostatic discharge. Precautions should be taken in handling, die attachment, and bonding to assure that Maximum Ratings are not exceeded as a result of electrical discharge.
- 3) Chips have been cleaned and are ready for die attachment. DO NOT attempt to re-clean.
- 4) Assembly should be performed with parts no hotter than 300°C. All circuit components (such as resistors and capacitors) should be assembled completely before the FET is die attached. Assembly should be performed as quickly as possible. In general, no chip should be left at 300°C for over 2 minutes.
- 5) Die attach with clean AuSn alloy under forming gas at 280 to 300°C. Scrub chip down with tweezers. Thermal resistance is critically dependent on this operation.
- 6) Thermasonic wedge bonding is recommended. A .0015 in. bond flat wedge at 125 to 150°C should be used with a heater stage temperature of 200 to 225°C. Apply 15 to 20 grams of bond force to .001 in. diameter gold wire with an elongation of 2 to 5 %.
- 7) Store in clean, dry, inert environment such as nitrogen at room temperature.
- 8) CAUTION: Handling of chips other than as specified above may cause permanent damage.

## **Idss Bin Selection**

Each die is DC probed at the wafer level. DC probe pass/fail limit specifications are published in the individual device data sheets. If a die fails to meet a DC specification it is inked, and therefore automatically scrapped. If a die fails to meet its DC specifications, MwT electronically records and archives its Idss value by location on wafer. After the wafer is scribed and broken, each die is automatically picked from expanded tape and placed into a die container according to its Idss value. All dies within a container will have the same measured on-wafer Idss values within a given Idss Bin range. Please refer to individual data sheets for Idss Bin ranges. Shaded Idss Bins indicate ranges where only small quantities may be available. These Bins should not be specified for volume production applications.

For commercial grade, level 1 visual die, a price premium applies to orders specifying less than 6 consecutive Idss Bins. For level 3 visual, the premium applies to orders specifying less than 3 consecutive Idss Bins.

## **Idss Bin Accuracy**

Due to the effects of temperature, dc loading and probe tip varnishing, the IDSS from the "on wafer" probing of any MwT device may differ after it has been attached to a proper heat sink and tested in an RF or DC circuit.

Because of the aforementioned effects, the IDSS distribution may typically deviate as much as +/- 1 Bin range from the Idss shown on the label of each die container but will not vary by more than +/- 2 Bins.