

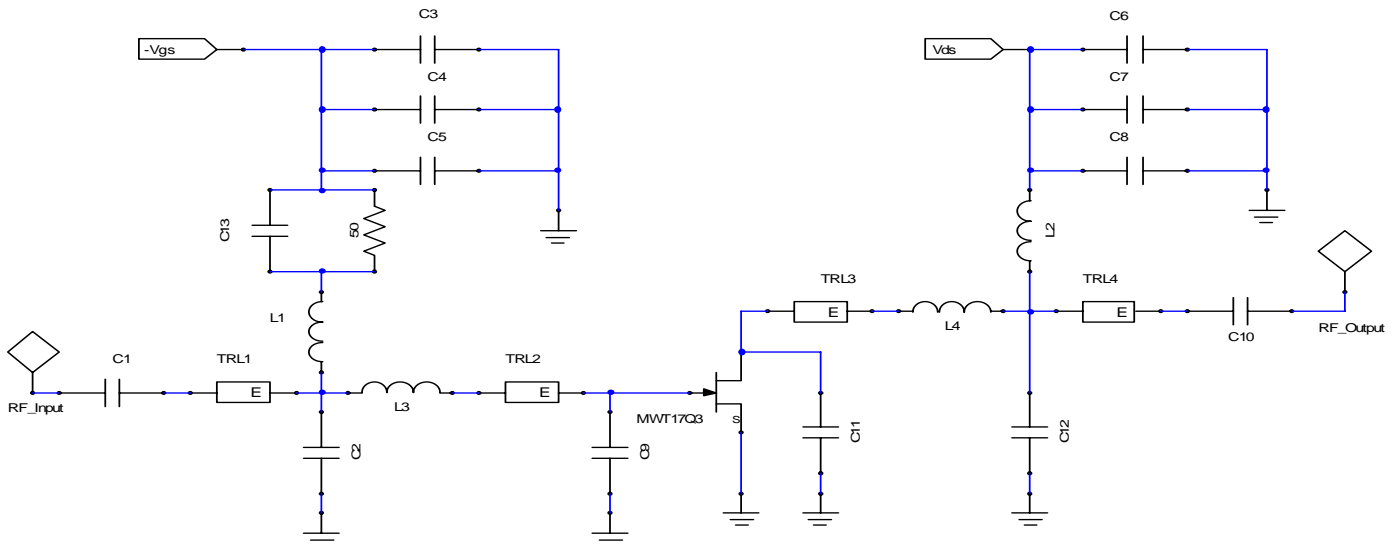
# Reference Circuit For Low Noise Applications

Typical RF Performance bias at  $V_{ds}=5V$ ,  $I_{ds}=200mA$ ,  $T_a=25^\circ C$

Parameter	Units	Typical Data			
Test Frequency	MHz	870-960	1800-2100	2400-2600	3400-3600
Gain	dB	18	16	13	10
Output IP3	dBm	43	43	44	44
Noise Figure(*)	dB	0.8	1.3	1.5	2.2

\* NF measure at  $I_{ds}=100mA$

## Circuit Schematic:

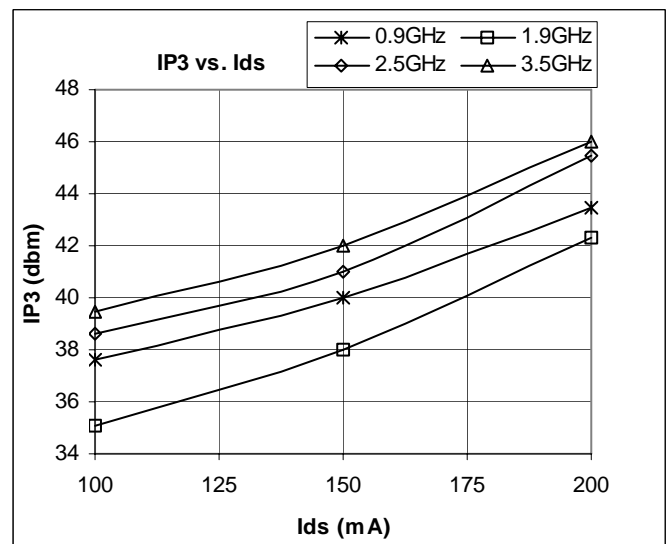
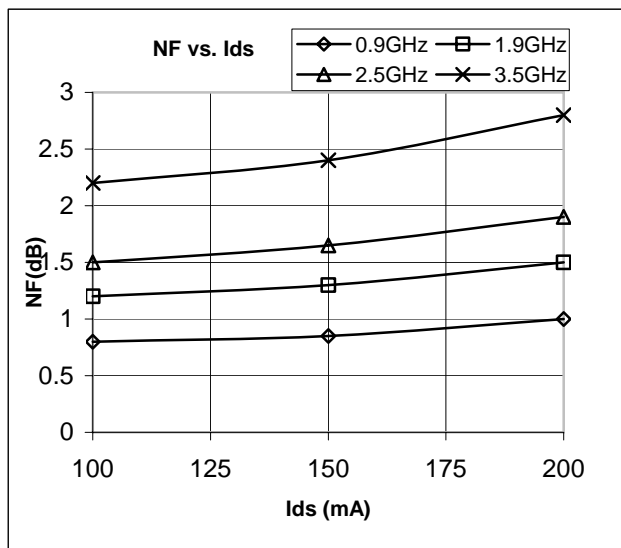


1. This low noise amplifier circuit will require balanced configuration in order to achieve good return loss.
2. The information and the reference circuit provided in this note are intended to show the capability of the MwT-17Q3 packaged FET and help customers to use the device in their designs for low noise applications.

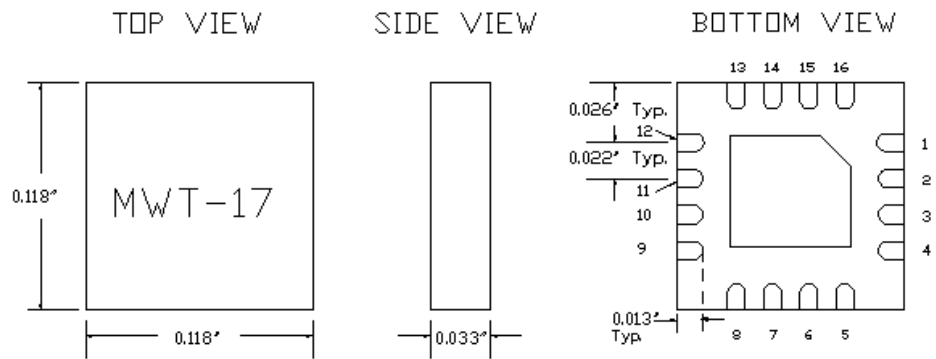
#### Bill of Material

Reference Designator	Value				Unit	part	Size
	0.87 – 0.96	1.8 – 2.1	2.4 – 2.6	3.4 – 3.6			
C5, C8	100	100	100	100	pF	Chip capacitor	0603
C4, C7	1000	1000	1000	1000	pF	Chip capacitor	0603
C3, C6	0.1	0.1	0.1	0.1	uF	Chip capacitor	1206
C1	100	22	4.7	2.2	pF	Chip capacitor	0402
C2	0.8	2	1.5	1.5	pF	Chip capacitor	0402
C9	NI	NI	NI	2.0	pF	Chip capacitor	0402
C10	100	22	4.7	3.3	pF	Chip capacitor	0402
C11	NI	NI	NI	1.2	pF	Chip Capacitor	0402
C12	1.6	NI	1.2	1.0	pF	Chip capacitor	0402
C13	NI	47	NI	NI	pF	Chip capacitor	0402
L1	100	82	18	10	nH	Chip Inductor	0603
L2	100	82	18	15	nH	Chip Inductor	0603
L3	6.8	0	0	0	nH	Chip Inductor	0603
L4	5.1	0	0	0	nH	Chip Inductor	0603
R1	50	50	50	50	Ohm	Chip Resistor	0603
TRL1	15	21	30	35	Deg.	50 Ohm TRL	
TRL2	0	16	20	25	Deg.	50 Ohm TRL	
TRL3	0	16	20	25	Deg.	50 Ohm TRL	
TRL4	15	21	30	35	Deg.	50 Ohm TRL	
Q	MwT-17Q3	MwT-17Q3	MwT-17Q3	MwT-17Q3		MESFET	QFN

NI: Not Installed



## MWT-17Q3 OUTLINE



Gate : 2 & 3 (both required)  
 Drain : 10 & 11 (both required)  
 Source : Backside ground  
 Ground Pad : 0.070" X 0.070" Typ.