APPLICATION		REVISIONS			
NEXT ASSEMBLY	USED ON	LTR.	DESCRIPTIONS	DATE	APPROVED
		A	RELEASE/ECN#5346	5/28/98	J. BRUNO
		B	REVISED/ECN#5984	11/26/02	S. COOPER
		C	REVISED/ECN#6279		

SEMICONDUCTOR STANDARD
VISUAL INSPECTION SPECIFICATIONS
FOR MwT GaAs FETs LEVEL 1

REVISION STATUS OF SHEETS **ENGINEERING DRAWING**

REV.																				
SHEET	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
REV.	C	C	C	C	C															
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES

TOLERANCES

fractions	decimals	angles
±	xx ±	±
	xxx ±	

All surfaces √ except as noted

MATERIAL:

Note: Deburr and break all sharp edges except as noted.

APPROVALS	SIGNATURE AND DATE
DRAWN BY	D. ANDERSON 5/19/98
PROJ. ENG.	J. BRUNO 5/26/98
MFG. ENG.	J. BRUNO 5/26/98
Q.A.	C. BECK 5/28/98

STAMP STATUS:

MICROWAVE TECHNOLOGY, INC.
Fremont, California, U.S.A.

SEMICONDUCTOR STANDARD VISUAL INSPECTION SPECIFICATIONS FOR MwT GaAs FETs LEVEL 1

SIZE	CODE IDENT NO.		
A	**6Y341**	**7-20005**	**C**
DO NOT SCALE THIS DRAWING		SHEET 1 of 5	REV.

VISUAL INSPECTION SPECIFICATIONS FOR MwT GaAs FETs LEVEL 1

TABLE OF CONTENTS

4.0 PURPOSE:

The purpose of these specifications is to specify the visual inspection criteria for MwT GaAs FETs, Level 1 to detect and remove transistor die with defects that could lead to device failure during application.

5.0 REQUIREMENTS:

.1 Electrostatic Discharge

The devices under test are very sensitive to electrostatic discharge (E.S.D.) and all appropriate E.S.D. precautions required will be utilized during handling, testing and screening (see MwT 3-00065).

2.2 Viewing Conditions

All chips to be inspected in bright field at 50X magnification. Chips are to be viewed with the GaAs surface sufficiently normal to the viewing direction to give bright reflection of the illumination.

3.0 OVERVIEW

Not Applicablle.

4.0 EQUIPMENT

Item	Description	Manufacturer	Model
1	Wrist Strap	3M	#2066 or equivalent
2	Static free work surface	---	---
3	Microscope, Grounded	---	---

5.0 TERMS AND DEFINITIONS

Channel Area	An area between edges fo overlay metal on drain and source within mesa boundary
Passivation	The layer(s) of transparent insulating material that covers the active circuit area, with the exception of bounding pad areas.
Scratch	Any tearing defect including probe marks in the surface for the metallization.

Smear	A track of metal caused, for example, when a probe slips off a pad and pushes onto areas outside the pad.

6.0 SAFETY:

Not Applicable.

7.0 PROCESS CONTROLS:

Not Applicable

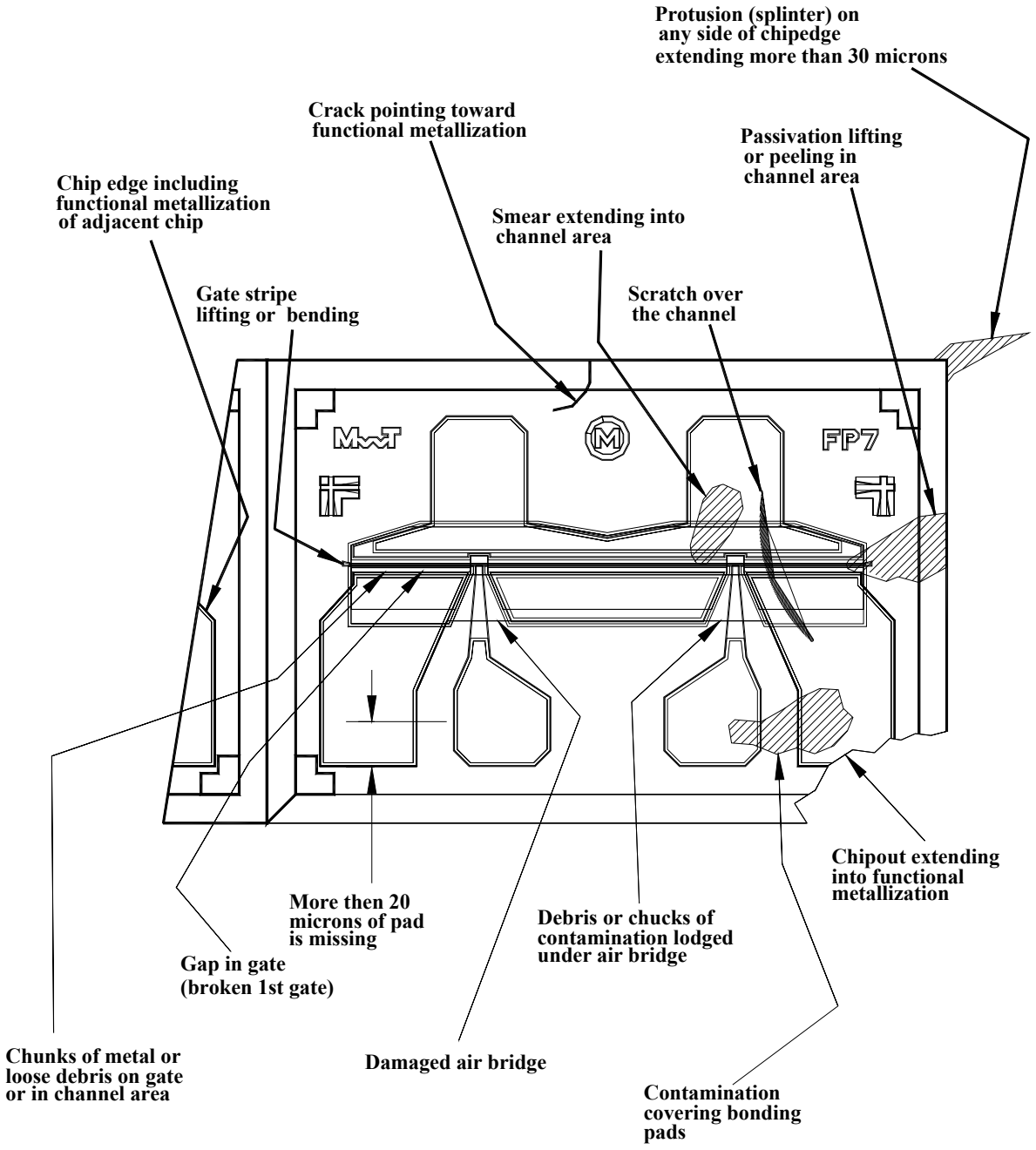
8.0 INSPECTION CRITERIA:

No device is acceptable that exhibits any of the following (see Figure 1 for reference):

a) Scratch over the channel area.
b) Smear extending into channel area.
c) More than 20 microns of pad missing
d) Contamination covering bonding pads
e) Crack pointing toward functional metallization.
f) Chipout extending into functional metallization.
g) Chip edge including functional metallization of adjacent chip.
h) Gate stripe lifting.
i) Passivation lifting or peeling in channel area.
j) Protusion on any side of chip edge extending more than 30 microns (splinters)
k) No chunks of metal or loose debris of gate or in channel area.
l) No debris or chunks of contamination lodged under air bridge.
m) No damage to air bridge.
n) No Gap in gate (broken 1st gate)

9.0 FIGURES:

Figure 1



Microwave Technology, Inc.	7-20005 Rev. B
Fremont, California, U.S.A.	Sheet 5 of 5

Figure 1

MicroWave Tevchnology, Inc	Filename	Code Ident. No.	7-20005 Rev. C
Fremont, California	7-20005C	6Y341	Sheet 5 of 5