APPLICATION		REVISIONS			
NEXT ASSEMBLY	USED ON	LTR.	DESCRIPTIONS	DATE	APPROVED
		A	RELEASE/ECN#5345	5/07/98	T. NAKAMURA
		B	REVISED/ECN#5518	11/8/99	R. C. Hamilton

SEMICONDUCTOR STANDARD VISUAL INSPECTION SPECIFICATIONS FOR MwT GaAs FETs LEVEL 3

REVISION STATUS OF SHEETS **ENGINEERING SPECIFICATIONS**

REV.																				
SHEET	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
REV.	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B					
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	APPROVALS	SIGNATURE AND DATE	MICROWAVE TECHNOLOGY, INC. Fremont, California, U.S.A.
TOLERANCES	DRAWN BY	D. LUJAN /04/98	
fractions ± / decimals xx ± xxx ± / angles ±	PROJ. ENG.	T. NAKAMURA 5/07/98	SEMICONDUCTOR STANDARD VISUAL INSPECTION SPECIFICATIONS FOR MwT GaAs FETs LEVEL 3
	MFG. ENG.	P. PACADA 5/07/98	
	Q.A.	S. COOPER 5/13/98	
All surfaces √ except as noted			
MATERIAL:	RELEASED		SIZE: A / CODE IDENT NO.: 6Y341 / 7-20007 / B
Note: Deburr and break all sharp edges except as noted.	DO NOT SCALE THIS DRAWING		SCALE: NONE / SHEET 1 of 15 / REV.

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VISUAL INSPECTION SPECIFICATIONS FOR MwT GaAs FETs LEVEL 3

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1.0 PURPOSE

The purpose of these specifications is to specify the visual inspection criteria for MwT Level 3 GaAs FETs to detect and remove transistor die with defects that could lead to device failure during application.

2.0 REQUIREMENTS

2.1 Electrostatic Discharge

The devices under test are very sensitive to electrostatic discharge (E.S.D.) and all appropriate E.S.D. precautions required will be utilized during handling, testing and screening. (See MwT 3-00065)

2.2 Viewing Conditions

All chips to be inspected in bright field at a magnification range from 75X to 500X. Chips are to be viewed with the GaAs surface sufficiently normal to the viewing direction to give bright reflection of the illumination.

2.3 Standards Compliance

The following visual inspection specifications meet the intent of MIL-STD-883, Method 2010, Test Condition B.

3.0 OVERVIEW

Not Applicable.

4.0 EQUIPMENT

Item	Description	Manufacturer	Model
1	Wrist Strap	3M	#2066 or equivalent
2	Static free work surface	---	---
3	Microscope, Grounded	---	---

5.0 TERMS AND DEFINITIONS

Abrasion	A change in the surface morphology of the metal which does not indicate tearing or significant (greater than 50%) reduction of the metal thickness.
Active Circuit Area	All areas enclosed by the perimeter of functional circuit elements, operating metallization or any connected combinations thereof excluding beam leads.
Air Bridge	A raised layer of metallization used for interconnection that is isolated from the surface of the element.
Crazing	The presence of numerous minute cracks in the reference material, (e.g., glassivation crazing).
Channel Area	An area between edges of overlay metal on drain and source within mesa boundary as defined by hash lines (see Figure 1).
Foreign Material	Any material that is foreign to the microcircuit or package, or any nonforeign material that is displaced from its original or intended position within the microcircuit package.
Passivation	The layer(s) of transparent insulating material that covers the active circuit area, with the exception of bonding pad areas.
Scratch	Any tearing defect including probe marks in the surface of the metallization.
Smear	A track of metal caused, for example, when a probe slips off a pad and pushes onto areas outside the pad.

6.0 SAFETY

Not Applicable.

7.0 PROCESS CONTROLS

Not Applicable.

8.0 INSPECTION CRITERIA

No device is acceptable that exhibits any of the following:

8.1 Ohmic Contact Metallization

See Figure 1 for reference.

Channel Area:

a) Deformation toward gate exceeding 0.5 microns.
b) Deformation away from gate exceeding 0.5 microns and affecting more than 10% of channel width.
c) Peeling or cracking.

All Areas:

d) Deformation or misalignment causing the space between any two electrodes to be less than 50% of its intended width.
e) Deformation greater than 10 microns.

8.2 Gate Stripe

See Figure 2 for reference.

a) Stripe width less than 0.5 microns.
b) Void reduces metal greater than 50%.
c) Nodule greater than 1 micron or greater than 150% of gate stripe.
d) Incomplete trough between stripe edges within mesa boundaries.
e) No space between trough edge and stripe edge.
f) Flag at end of stripe not extending beyond mesa edge.
g) Scratch or abrasion.
h) No peeling.
i) No bending greater than 0.5 microns.

.3 Overlay and Interconnect Metallization

See Figure 3 for reference.

Within 10 microns of Channel Area:

a) Overlay metal extending beyond ohmic metal edge in area.

Bonding Pad:

b) A scratch in the bonding pad area that exposes underlying material and reduces the metallization to less than 50% of the designed width.

All Areas:

c) Deformation greater than 10 microns.
d) Deformation reducing the space between two electrodes to less than 50% of its intended width.
e) Deformation or void reducing the width of conducting path to less than 50% of its intended width.
f) Scratch or void affecting more than 25% of the conductor width.
g) Smear, away from channel area, extending more than 25 microns from any operating metallization.
h) Smear reducing the space between two electrodes to less than 50% of its intended width.
i) Protrusion higher than 10 microns.
j) Peeling of functional metallization.

8.4 Air Bridge Metallization

See Figure 4 for reference.

a) Hole not centered within 1.5 microns of its intended position with respect to both gate and air bridge metallization.
b) Deformation of hole reducing its area by more than 50% of its intended area.
c) Deformation reducing gap between air bridge metal edges to less than 50% of intended size.
d) Mechanical damage to an air bridge where no visible separation between the air bridge and the underlying metallization exists.

8.5 Excess Metal

See Figure 4 for reference.

a) Excess metal coming closer than 5 microns of any operating metallization.
b) Excess metal reducing any insulating gap to less than 50% of its intended size.

8.6 GaAs Surface

See Figures 5 and 6 for reference.

Within 10 microns of Channel Area:

a) Deformation or misalignment of mesa edges by more than 1.5 microns.

All Areas:

b) Unintended mesa island and deformity of mesa edge reducing any electrode gap by more than 50%.
c) Deformity of mesa edge by more than 10 microns from electrode edge.

8.7 Contamination

Contamination consists of particles, stains, ink or corrosion. See Figures 5 and 6 for reference.

Channel Area:

a) Contaminant in the gap between gate stripe and ohmic contact metal.

Bonding Pad:

b) Pad size less than or equal to 2 by 2 micron, No contaminantes.
c) Pad size greater than 2 by 2 micron, contaminante affecting more than 50% of bonding area.

Air Bridge:

d) Contaminant or particle lodged against the edge or under an air bridge where it crosses over other metallization.

All Areas:

e) Contaminant bridging gap between active areas or functional Metallization.
f) Contaminant or particle higher than 10 microns.

8.8 Chip Irregularities

See Figure 7 for reference.
a) Chipout extending more than 30 microns in from chip edge.
b) Chipout coming closer than 2.5 microns from any active area or functional metallization.
c) Chip edge coming closer than 10 microns from any functional metallization.
d) Chip edge lying beyond inner edge of street marker of adjacent chip.
e) Protrusion at the bottom of chip, on any side, extending more than 25 microns from chip edge.
f) Crack longer than 125 microns.
g) Crack coming closer than 2.5 microns to any active area or functional metallization.
h) Crack longer than 25 microns pointing toward an active area or functional metallization.

8.9 Passivation

See Figure 8 for reference.

Channel Area:

a) Crack or crazing.
b) Void or blister extending into or located within any part of the ohmic contact gap.

All Areas:

c) Void or blister larger than 5 microns in diameter.
d) Lifting or peeling.

9.0 FIGURES

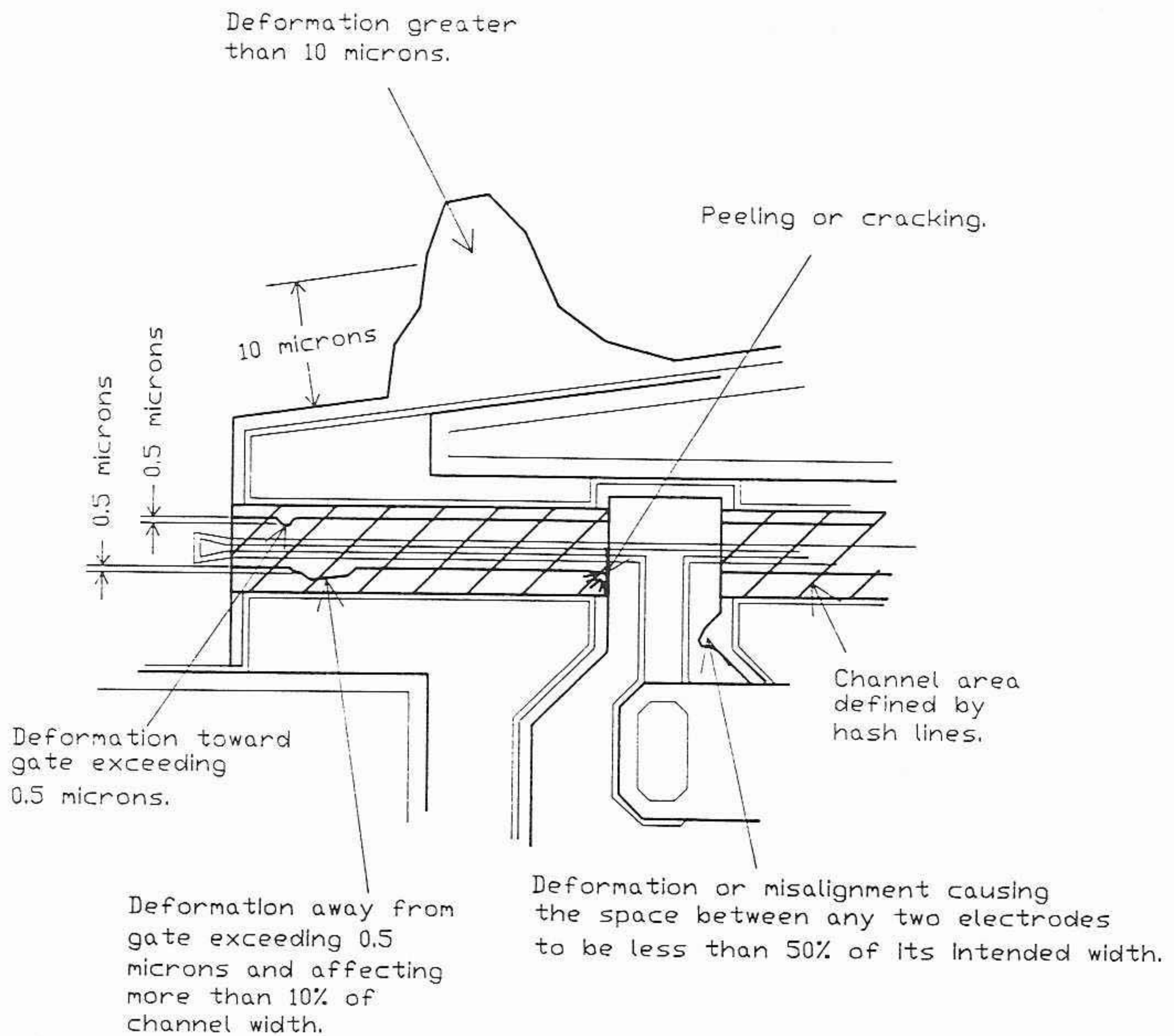


Figure 1 Ohmic Contact Metallization

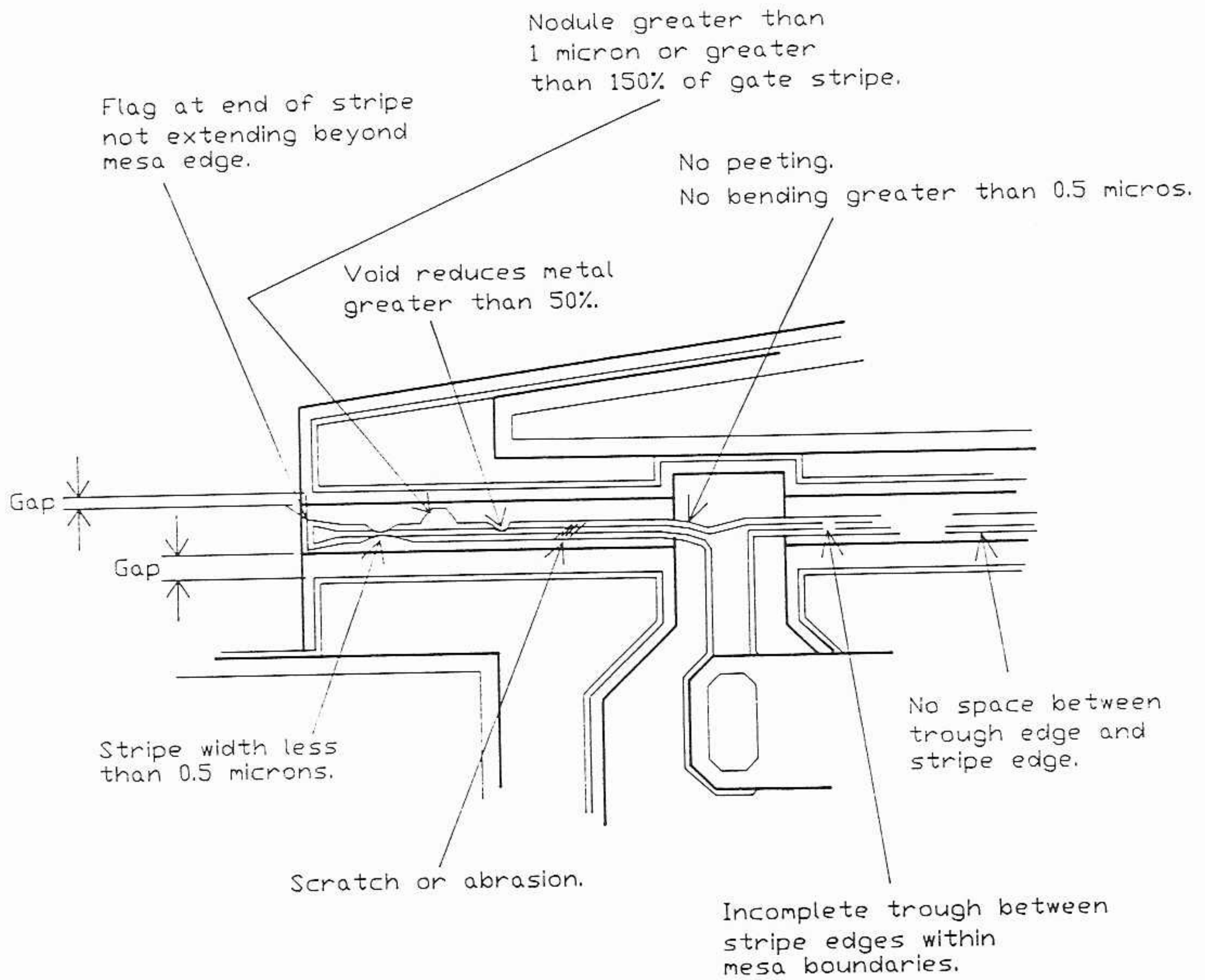


Figure 2 Gate Stripe

Deformation reducing the space between two electrodes to less than 50% of its intended width.

A scratch in the bonding pad area that exposes underlying material and reduces the metallization to less than 50% of the designed width.

Void reducing width of conducting path to less than 50% of its intended width.

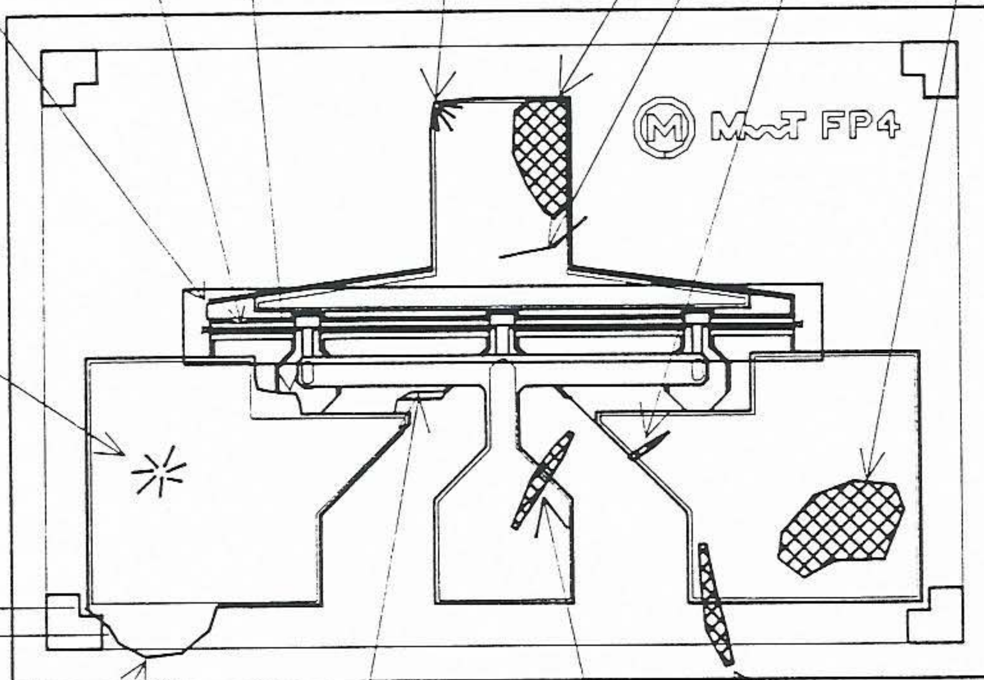
Scratch affecting more than 25% of the conductor width.

Overlay metal extending beyond ohmic metal edge in area within 10 microns of channel.

Peeling of functional metallization.

Void affecting more than 25% of the conductor width.

Protrusion of metal higher than 10 microns.



10 microns

Deformation greater than 10 microns.

Smear, away from channel area, extending more than 25 microns from any operating metallization.

Smear reducing electrode gap to less than 50% of intended width.

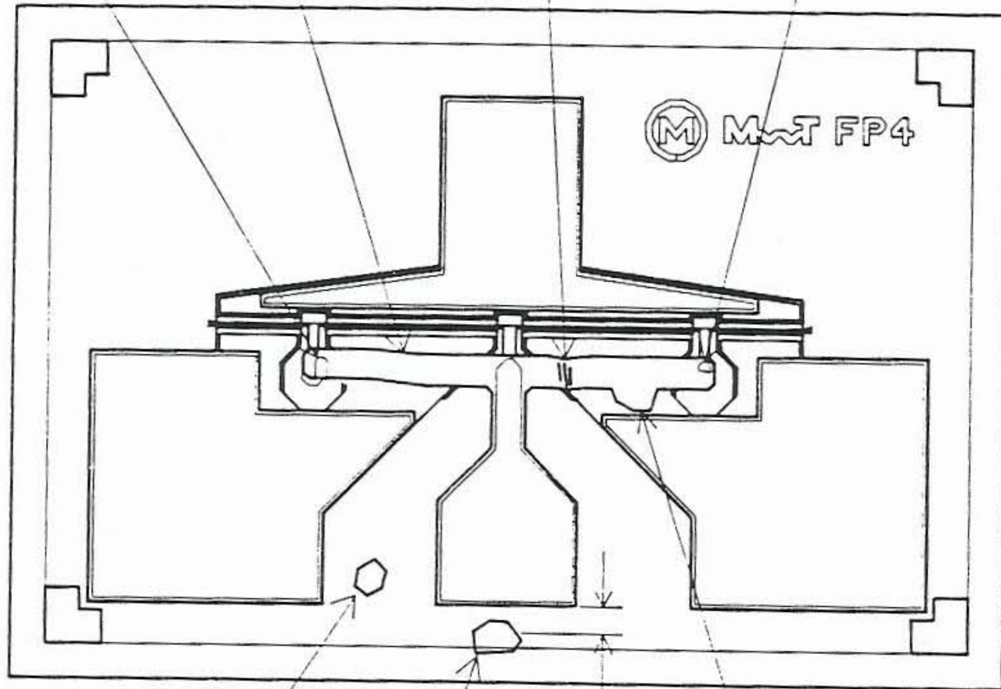
Deformation reducing width of conducting path to less than 50% of its intended width.

Figure 3 Overlay and Interconnect Metallization

Hole not centered within 1.5 microns of its intended position with respect to both gate and air bridge metallization.

Deformation of hole reducing its area by more than 50% of its intended area.

Mechanical damage to an air bridge where no visible separation between the air bridge and the underlying metallization exists.



5 microns

Excess metal reducing insulating gap to less than 50% of intended size.

Deformation reducing gaps between air bridge metal edges to less than 50% of its intended size.

Excess metal coming close than 5 microns of operating metallization.

Figure 4 Air Bridge Metallization and Excess Metal

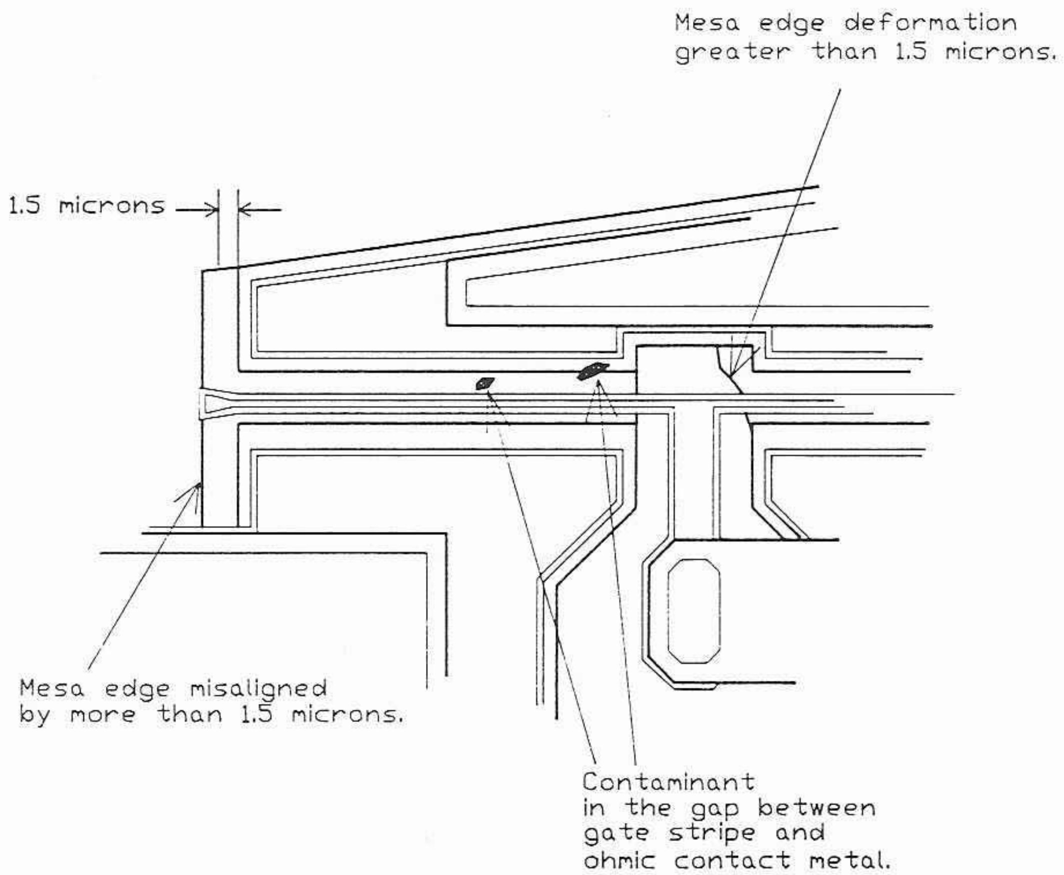


Figure 5 GaAs Surface and Contamination- Channel Area

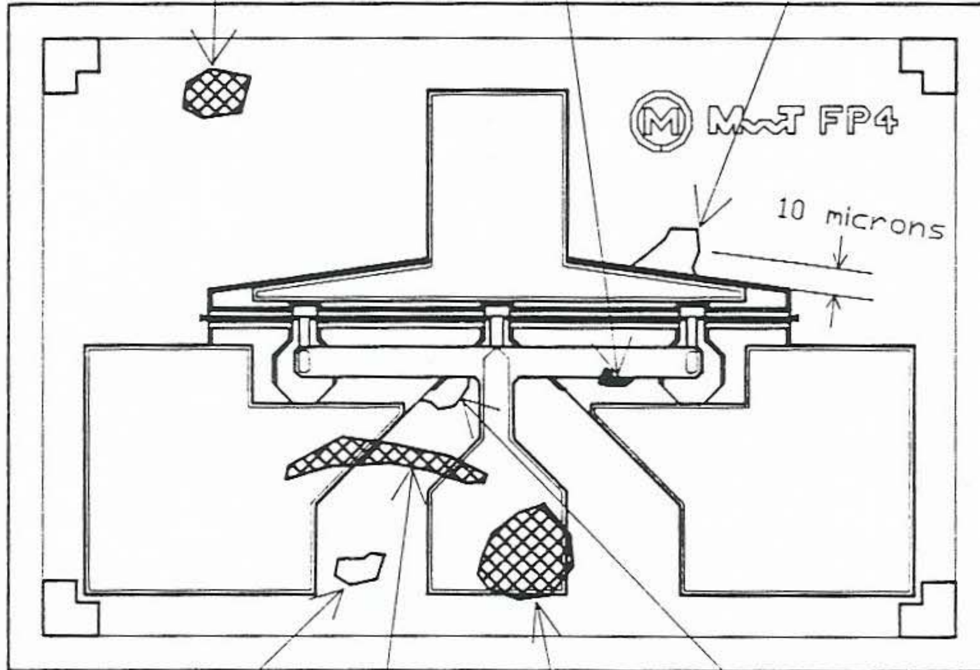


Figure 6 GaAs Surface and Contamination - All Area

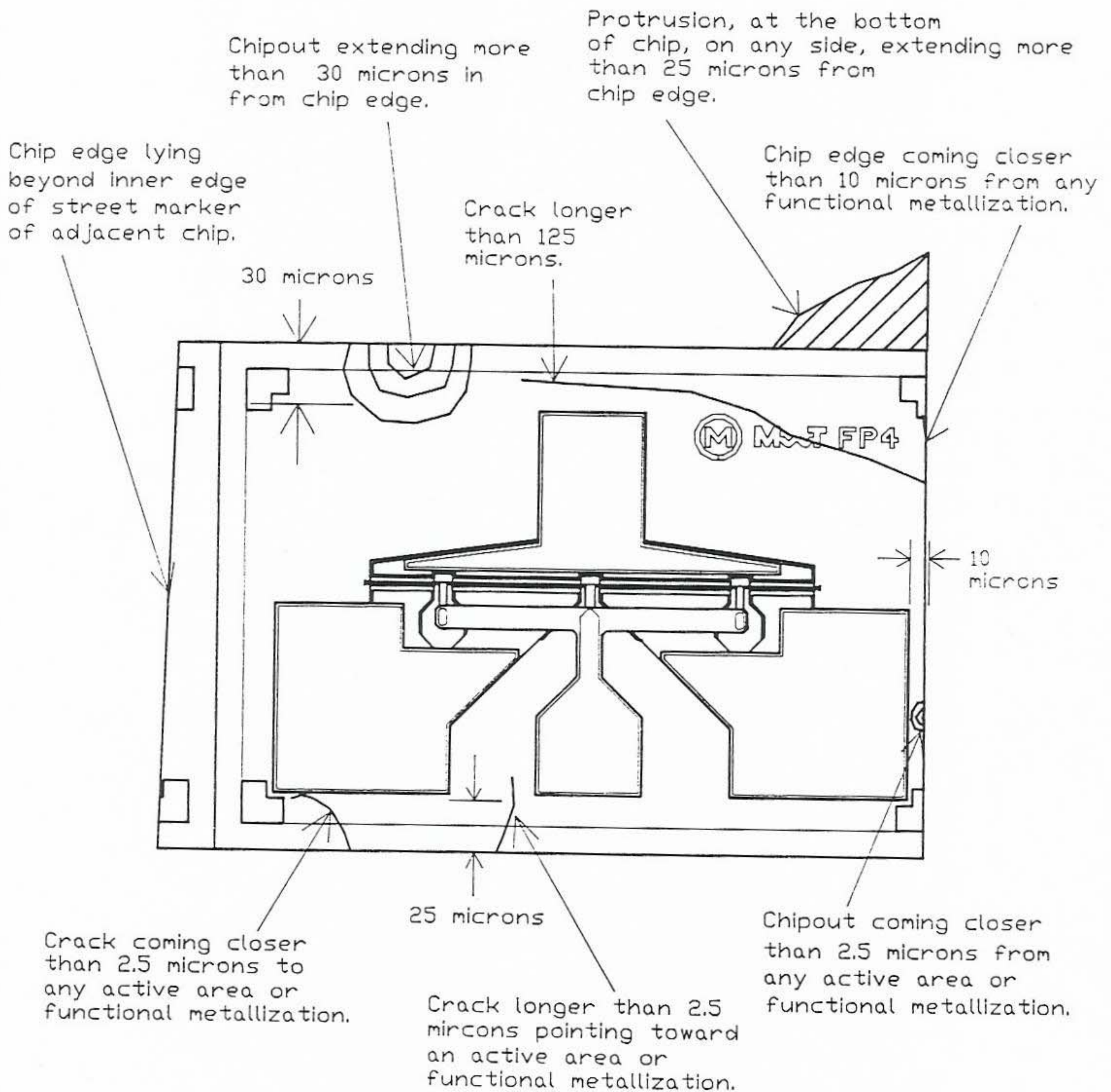


Figure 7 Chip Irregularities

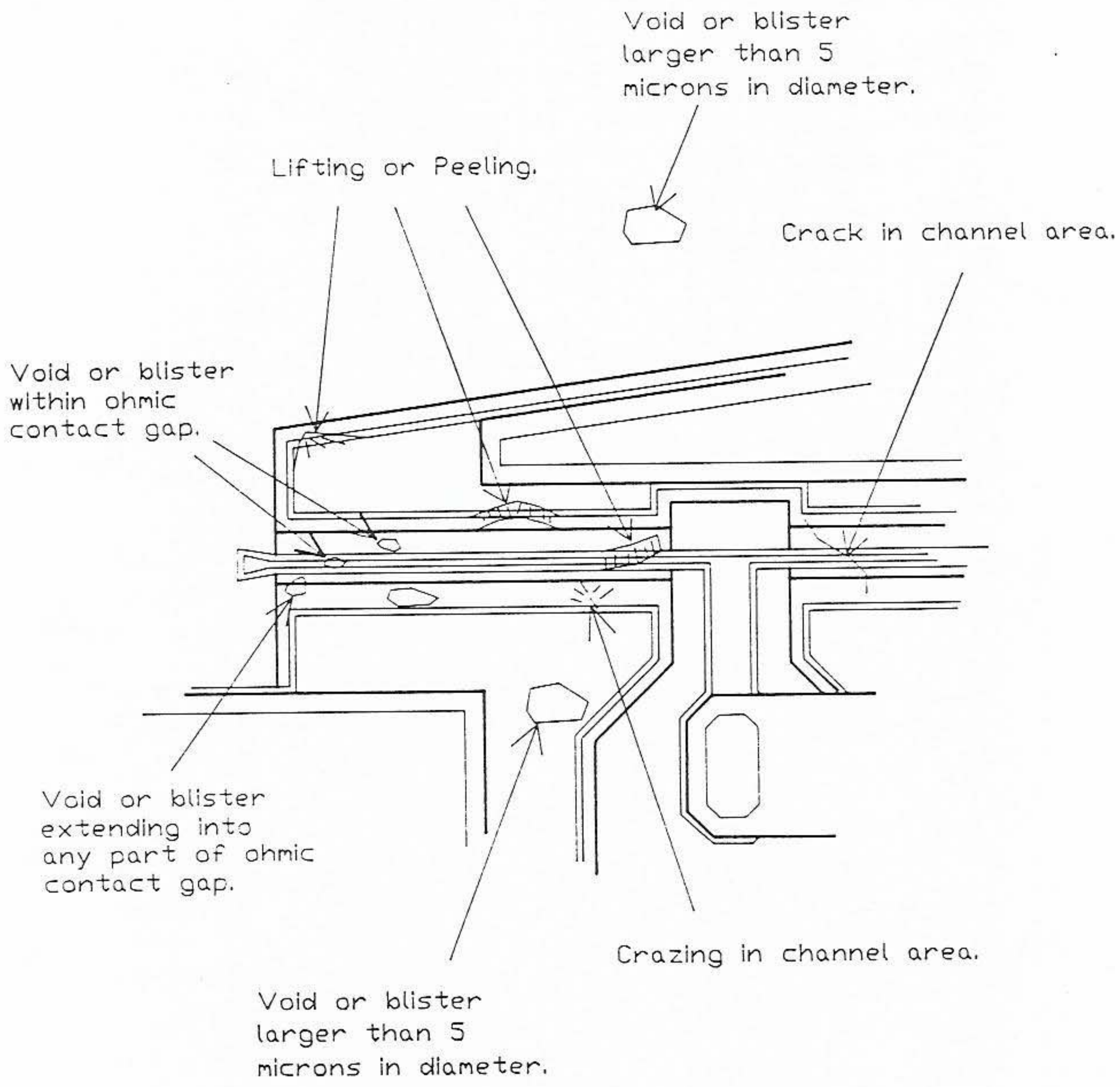


Figure 8 Passivation